# EXPERIMENTALLY VALIDATED MULTISCALE THERMAL MODELING OF ELECTRIC CABINETS

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Mechanical Engineering

Georgia Institute of Technology
December 2008

# EXPERIMENTALLY VALIDATED MULTISCALE THERMAL MODELING OF ELECTRIC CABINETS

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Date Approved: August 15, 2008

## ACKNOWLEDGEMENTS

First of all, I would like to express my sincere thanks to Professor Yogendra Joshi, for his support and guidance during my doctoral studies. He has shaped me as a researcher and influenced me as a thinker. I am grateful for his insight and career advice, but most of all his confidence in me.

I would also like to express my appreciation to my dissertation committee members, Dr. Zhuomin Zhang, Dr. Samuel Graham, Dr. Martha G. Gallivan, and Dr. P. K. Yeung, for their time and efforts in reviewing the dissertations and their valuable suggestions.

My sincere gratitude goes to ONR for their financial support. I would also like to thank the director of the ONR research project, Dr. Mark Spector, for his helpful advices and encouragements.

My sincere gratitude also goes to all my current and former colleagues, especially, Carter Dietz, Graham Nelson, Ludovic Burton, Emad Samadiani, Shawn Shields, Ethan Cruz, Ashish Sinha, Dr. Jeff Rambo, Dr. Yoon Jo Kim for the valuable, or otherwise interesting, discussions we have had concerning this and many other research topics.

I am also grateful to the staff at the Packing Research Center, the Machine Shop and Electronics Shop of Mechanical Engineering for their support of the manufacturing, assembly, and test of the test vehicle.

Last but not least, I would like to express my deepest gratitude to my family. I would like to thank my parents for their unconditional and eternal love and support. Their encouragement is always with me and has given me the strength to complete this work. Special thanks to my loving wife, Lijun Zu, for her enthusiasm in life and work and for her love and patience throughout the years.

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# LIST OF SYMBOLS

| | |
|---|---|
| $a, b, c$ | modal coefficients |
| $\boldsymbol{a}$, $\boldsymbol{b}$, $\boldsymbol{c}$ | modal coefficients matrix |
| $A$ | cross-sectional area, $m^2$ |
| $B_i$ | Biot Number |
| $c_p$ | specific heat, J/kg-K |
| $c_\mu$ | $k-\varepsilon$ model coefficient |
| $E$ | eigenvalue energy spectra |
| $F$ | flow rate function |
| $G$ | goal flow rate function |
| $H^2$ | Hilbert space |
| $k_b$ | Boltzmann constant, J/K |
| $K$ | pressure loss coefficient |
| $\mathbf{n}$ | normal direction |
| $N$ | number of TE elements |
| $\mathbf{P}$, $\mathbf{T}$, $\mathbf{U}$ | observation ensemble matrix |
| $P$ | pressure, $N/m^2$ |
| $Pr_t$ | turbulence Prandtl number |
| $Q$ | heat generation, W |
| $q_e$ | electric charge, Coulomb |
| $r$ | correlation coefficient |
| $R$ | subspace of Hilbert space |
| $Re_L$ | Reynolds number |

| | |
|---|---|
| $S$ | momentum source term |
| $T$ | temperature, K |
| $\mathbf{u}$ | velocity field, m/s |
| $u$ | horizontal velocity, m/s |
| $U$ | ensemble matrix |
| $V$ | flow field variables, $P$, $T$, $\mathbf{u}$ |
| $w$ | width, m |
| $\Gamma$ | boundary |
| $\kappa$ | thermal conductivity, W/m-K |
| $\lambda$ | eigenvalue |
| $\nu$ | kinetic viscosity, $m^2/s$ |
| $\Pi, \Phi, \Psi$ | POD modal space |
| $\rho$ | density, $kg/m^3$ |
| $\varphi, \phi, \psi$ | POD mode |
| $\Omega$ | system domain |
| $\beta$ | weight coefficient of temperature modes |
| $\alpha$ | thermal diffusivity, $m^2/s$ |
| $I$ | electric current |
| $\mu$ | dynamic viscosity, kg/m-s |
| $h$ | convective heat transfer coefficient |

**Subscripts**

| | |
|---|---|
| $c$ | constant part of source term |
| $e$ | enclosure part |
| $eff$ | effective fluid property |
| $err$ | error |

| | |
|---|---|
| $f$ | full length |
| $h$ | heat flow |
| $l$ | TE element |
| $m$ | mass flow |
| $o$ | source |
| $p$ | slope of source term |
| $//$ | lateral |
| $\perp$ | transverse |
| $sp$ | spreading |
| $D$ | forward |
| $S$ | saturation |
| $app$ | approach |
| $b$ | base |

**Superscripts**

| | |
|---|---|
| $m$ | number of nodes |
| $n$ | number of modes |
| $obs$ | observations |
| $r$ | reconstructed solution |
| $s$ | number of complement modes |
| $t$ | desired solution |
| T | transpose |
| $'$ | complement subspace |
| - | matrix inverse |
| $\perp$ | orthogonal subspace |
| + | pseudo-inverse |

# LIST OF ABBREVIATIONS

| | |
|---|---|
| AlN | Aluminum Nitride |
| BCI | Boundary Condition Independent |
| BGA | Ball Grid Array |
| CFD-HT | Computational Fluid Dynamics and Heat Transfer |
| CFM | Cubic Feet per Minute |
| CM | Compact Model |
| CTE | Coefficient of Thermal Expansion |
| DC | Continuous Current |
| DCB | Direct Copper Bonding |
| DOF | Degree of Freedom |
| DSC | Double-Sided Cooling |
| FDM | Finite Difference Method |
| FEM | Finite Element Method |
| FNM | Flow Network Modeling |
| GPIB | General Purpose Interface Bus |
| HS | Heat Sink |
| IGBT | Insulated Gate Bipolar Transistor |
| ODE | Ordinary Differential Equation |
| PCB | Printing Circuit Board |
| PCM | Power Conversion Module |
| PDE | Partial Differential Equation |
| POD | Proper Orthogonal Decomposition |

| | |
|---|---|
| PODc | Complementary Proper Orthogonal Decomposition |
| PQFP | Plastic Quad Flat Package |
| PWB | Printing Wiring Board |
| SAC | Single-sided Forced Air Convection |
| SIMPLE | Semi-Implicit Method for Pressure-Linked Equations |
| SWC | Single-sided Water Cooling |
| TEC | Thermoelectric Cooler |
| TIM | Thermal Interface Material |
| TCU | Temperature Control Unit |
| UBM | Under Bump Metallization |
| UPS | Virtual Product Simulator |

# SUMMARY

Thermal characterization of electronic cabinets is becoming increasingly important, due to growing power dissipation and compact packaging. Usually, multiple length scales of interest and modes of heat transfer are simultaneously present. A steady reduced order thermal modeling framework for electronic cabinets was developed to provide an efficient method to model thermal transport across multiple length scales. This methodology takes advantage of compact modeling at the chip or component level and reduced order modeling at subsystem and cabinet levels.

Compact models, which were incorporated into system level simulation, were created for components, and reduced order models (ROMs) were developed using proper orthogonal decomposition (POD) for subsystems and system. An efficient interfacial coupling scheme was developed using the concept of flow network modeling to couple the heat and mass flow rates and pressure at each interface, when interconnecting ROMs together to simulate the entire system. Thermal information was then subsequently extracted from the global modeling and applied to the component model for detailed simulation.

A boundary profile-matching scheme for ROM of each subsystem was developed to broaden the applicability of the multi-scale thermal modeling methodology. The output profiles of the subsystem upstream can be transferred to the input profiles of the subsystems downstream by adding necessary flow straightening ducts during the snapshots generation process.

A general method to create dynamic multi-layer compact models for components and modules was developed. These dynamic compact models were incorporated into enclosure level simulation. The dynamic reduced order model for the enclosure was developed using POD. The transient multi-scale thermal modeling approach was illustrated through an electronic enclosure with insulated gate bipolar transistor (IGBT) module.

The multiscale thermal modeling methodology presented here was validated through experiments conducted on a simulated electronic cabinet and the test vehicle with hybrid cooling technique. The latter incorporated double-sided cooling with hybrid forced air convection, thermoelectric cooling, and micro-channel liquid cooling. The overall multi-scale modeling framework was able to reduced numerical models containing $10^7$ DOF down to around $10^2$, while still retaining an approximation accuracy of around 90% in prediction of chip junction temperature rises, compared to measurements.

# CHAPTER 1

# INTRODUCTION

Electronic cabinets are used by industries and military for the housing of electronic devices. Based on the applications of these devices, there are three main classes of electronic cabinets, as shown in Figure 1.1. Data processing cabinets are widely used to house computational equipment, such as servers, storage units, and disk drivers. Telecommunication cabinets are typically used to accommodate phone switches, optical fiber switches, transmitters, and receivers, etc. Power electronic cabinets are mainly used for the storage of power conversion equipments and house power diodes, thyristors, diode rectifiers, and converters, etc.

(a) (b) (c)

Figure 1.1 Classification of electronic cabinets, (a) data processing cabinet, (b) telecommunication cabinet, (c) power electronic cabinet

For data processing cabinets housing servers with microprocessors, the number of transistors integrated per chip has grown dramatically according to Moore's law [1]. As a result, the total heat generation rates and device level heat fluxes have increased dramatically [2]. In 1990, a typical data processing cabinet dissipated approximately 1 kW of power [3], while today's cabinets with the same footprint may dissipate up to 30 kW, based on current server heat loads. The server power density has increased 300% during the decade from 1992 to 2002, with a projected annual increase of 5% over the next 4 years [4, 5], as shown in Figure 1.2. How to efficiently dissipate such a large amount of heat in electronic cabinets is a unique challenge for the thermal designers.

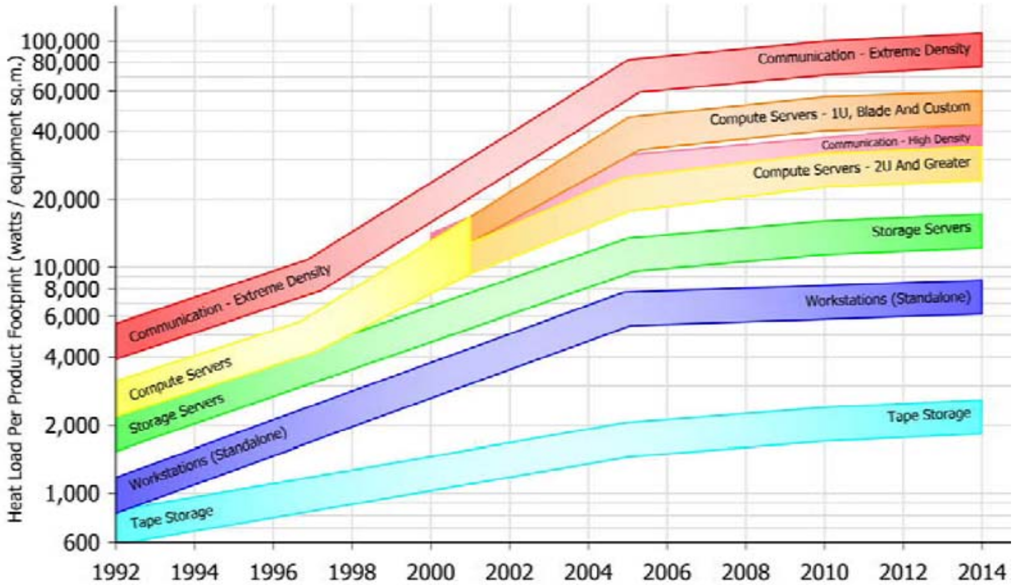


Figure 1.2 Power trend of server equipment [5]

## 1.1 Thermal Management of Electronic Cabinet

The thermal management community has focused intensively on cooling methods for electronic cabinets. Investigation of advanced cooling methods beyond forced air convection has been an active topic for research. In addition, the operation and maintenance cost of cooling devices are also important factors when selecting a cooling method. The state-of-the-art of cooling methods for electronic cabinets is described below.

### 1.1.1 Air Cooling

Air cooling is the most popular option, due to its easy equipment maintenance, low operation cost, and acceptable cooling efficiency. Natural convection is widely used in cooling of low power consumer electronics and potable electronic devices. Forced air convection is usually required for higher heat dissipation. Typically, three configurations of air-cooled electronic cabinets exist: cooled-plenum active cooling, perforated air flow cooling, and ducted active cooling, as shown in Figure 1.3 [6].

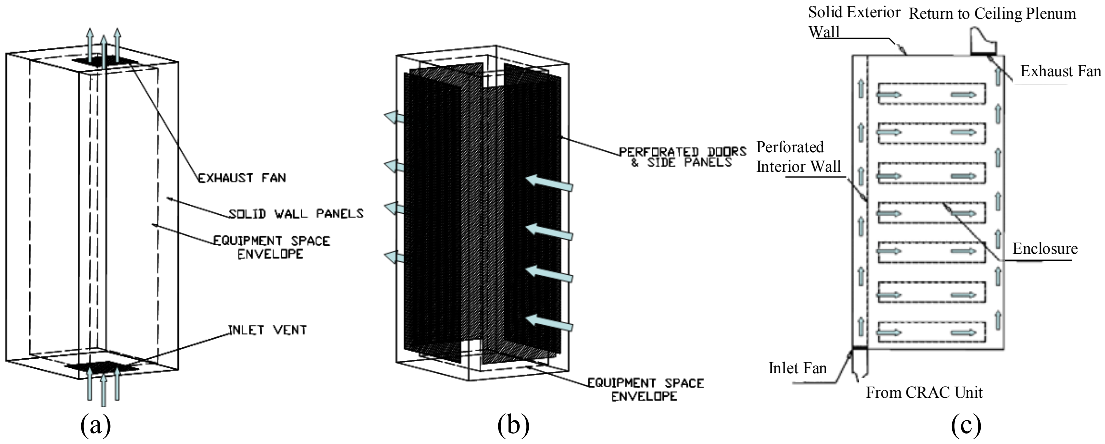



Figure 1.3 Configurations of air-cooled cabinet, (a) cooled-plenum active cooling, (b) perforated air flow cooling, (c) ducted active cooling

The cooled-plenum active scheme provides the cooling by cold air being drawn up into the cabinet from perforated tile in plenum directly below inlet vent. The hot air after taking the heat from the electronic devices inside the cabinet will exit the cabinet through the exhaust fan mounted at the top of the cabinet. For the perforated air flow cooling, the cold air flows across the system through perforations in walls and doors of the cabinet. This type of cooling is especially used in the 'Hot aisle-Cold Aisle' data center cooling methodology. The ducted active cooling configuration uses cold air ducted directly to the cabinet from the building's air-conditioning (AC) unit. The air flow is driven by the AC pressure, inlet fans and exhaust fans of the electronic cabinet. The exhaust of the cabinet is ducted directly to the AC unit, thus improving the cooling efficiency. The first cooling configuration is mainly utilized in cabinets with low heat dissipation, while the last two are widely utilized for heat loads up to 8.5kW [6].

### 1.1.2 Liquid Cooling

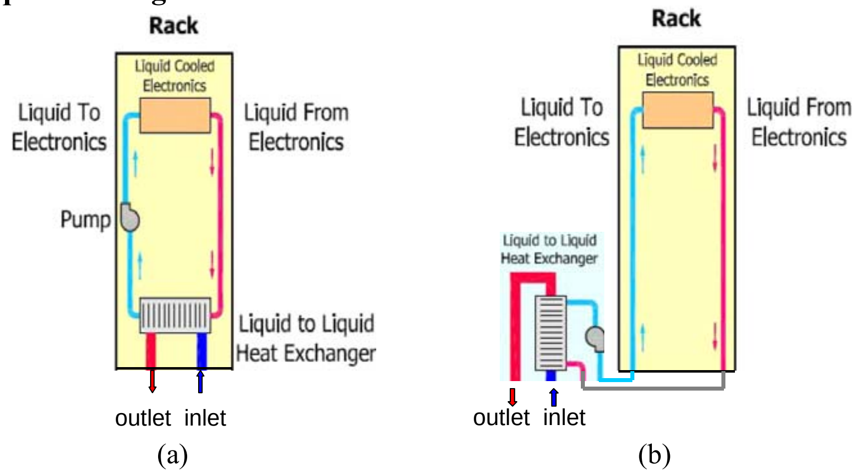
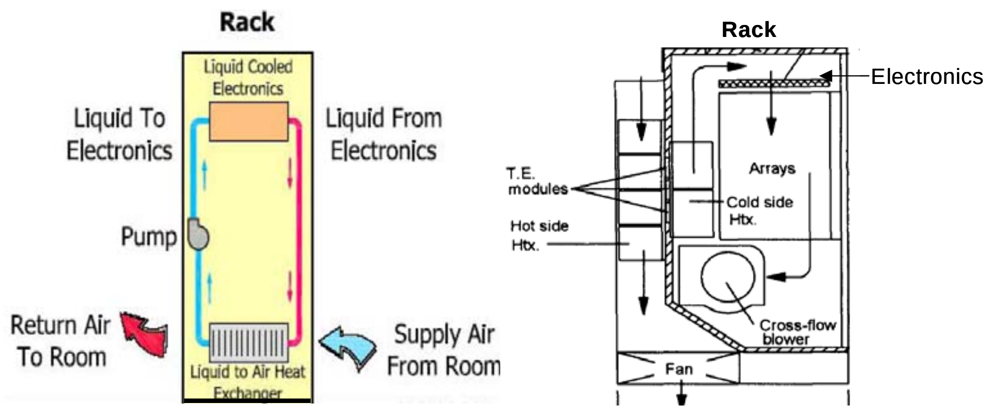



Figure 1.4 Configurations of liquid cooling, (a) internal liquid cooling loop, (b) external liquid cooling loop [5]

As heat loads continue to rise, so does the challenge of cooling with air due to the limits of heat sink/air moving device performance, and rack level acoustic limitations. Liquids, primarily because of their higher density and specific heat, are much more effective in the removal of heat than air, making liquid cooling a desirable choice for increase heat loads. Figure 1.4(a) shows a typical configuration liquid cooled cabinet, where the internal cooling loop utilizes a liquid to chilled water heat exchanger internal to the rack to dissipate the heat generation within the rack. Typically the liquid circulating within the rack is maintained above dew point to avoid any condensation of ambient moisture. Figure 1.4(b) depicts a design similar to Figure 1.4(a) but where some of the primary liquid loop components are housed outside the rack to permit more space within the rack for electronic components. The liquid cooling method is especially used for cabinets with high heat dissipation (up to 15kW or even higher).

### 1.1.3 Hybrid Cooling

Besides air and liquid cooling options, hybrid cooling is also increasingly utilized in a variety of applications. Figure 1.5(a) shows a liquid loop internal to the rack, where the exchange of heat with the room occurs with a liquid-to-air heat exchanger. The heat generated from the electronics is removed by the sealed air which circulates inside the rack. The cooling configuration is widely used in naval shipboard cabinets where the electronic devices need to be isolated from the ambient environment. Figure 1.5(b) shows a schematic of another hybrid air and thermoelectrically cooled cabinet. The air takes the heat from the electronics and circulates inside the rack, dissipating the heat to the thermoelectric (TEC) modules mounted to the sidewall. The air inside the plenum flows across the hot side of the TEC driven by the exhaust fan at the outlet of the plenum to remove the heat of the TEC modules.




(a) (b)

Figure 1.5 Hybrid cooling of rack, (a) air-liquid cooling [5], (b) air-thermoelectric cooling [7]

## 1.2 Motivation

Numerical simulation has been intensively used in thermal analysis of electronic cabinets [8-14], using a number of simplifications. However, multiple length scales of interest and modes of heat transfer are usually simultaneously present. For example, to achieve a 'chip-to-cabinet' thermal modeling capability, at least four decades of length scales need to be resolved simultaneously, as shown in Figure 1.6 [15]. Heat generated within the components is conducted across the chips, packages, and modules and is then removed at the boundaries by convection and/or radiation. The challenges of thermal characterization of electronic cabinets also result from complex geometry involved and large variations in thermophiscal properties commonly encountered in electronic packaging materials [16]. Consequently, large computing resources are required to resolve all length scales in order to provide accurate thermal modeling.

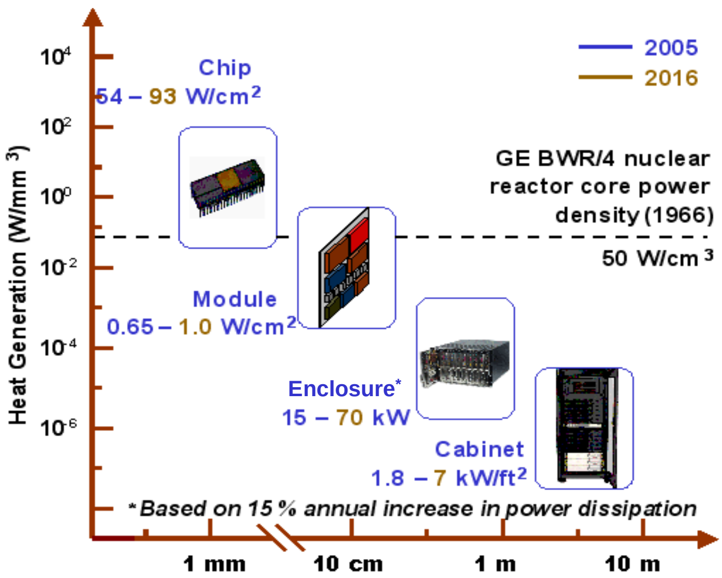



Figure 1.6 Volumetric heat generation rate projections across the microsystem packaging hierarchy [15]

In the past, thermal analysis in the microelectronics industry was typically focused on the performance at the component and module level by thermally isolating them from their surrounding environment. Numerical solution of the heat conduction equation was sought for the component and/or module with specified boundary conditions. In most cases, these boundary conditions ultimately rely on reference temperatures and convection heat transfer coefficients based on empirical correlations, which are strictly applicable to a limited range of conditions. The variation of cooling methods utilized in electronic cabinets imposes different boundary conditions on the electronic components and modules, resulting inaccuracies in thermal predictions.

The recently popular system level computational fluid dynamics/heat transfer (CFD/HT) simulations [17, 18] combine the analysis of flow environment with that of the heat transfer processes by solving the governing equations of continuity, momentum, and energy simultaneously. Such CFD/HT simulations have been conducted at the enclosure level [19-21]. While this approach provides more detailed information, it is computationally impractical to resolve all the length scales of interest for chips, components, and enclosures. One possible approach is to adopt simplified component and heat sink models [22-24]. In order to keep the computational time within a reasonable limit, in all these studies, details of the components and modules are ignored, with accuracy sacrificed accordingly.

With the advances in computing techniques, the CFD/HT simulations have been conducted at the cabinet level. Due to a much higher number of grid cells for the CFD/HT model of a cabinet than an enclosure, either highly simplified component and module models [13], or less components and modules [14] are adopted at the cabinet level simulation. Less detailed information on the components and modules is available through these approaches. To get significantly detailed information at component and enclosure levels, one possible approach is to conduct the experiments at cabinet level and extract the boundary conditions for the enclosure of interest, so that the detailed enclosure level simulation can be conducted [10]. However, experiments can not be conducted during the early design phase, rending such approach impractical for new cabinet design.

Given potential application at the cabinet level, the CFD/HT models are still limited due to the large amount of time invested in model construction and solution. The number of grid cells for a cabinet model is around 1 million by only considering certain important components [14]. For a 2-equation turbulence model in 3 dimensions, the finite volume method produces 7 degrees of freedom (DOF) per grid cell ($P, u, v, w, k, \varepsilon,$ and $T$) or around 7 million for the entire cabinet. A large amount of simulation time and memory space will be consumed for this CFD/HT model. It is therefore necessary to develop a systematic multi-scale method with the capability to efficiently model all levels of the packaging hierarchy in an integrated fashion under different scenarios. In other words, the multi-scale thermal modeling methodology being sought should be able to reduce the DOF of the system significantly, while maintaining reasonable simulation accuracy at each level.

### 1.3 Objectives and Overview of the Present Study

In the present study, a multi-scale methodology is developed for efficient thermal analysis of complex electronic cabinets under steady-state operation. This methodology distinguishes itself from conventional single level (cabinet, enclosure, and module/component level analysis) methods in that analyses of different levels are efficiently integrated through thermal information communication. As a result of this, detailed information across each level is available, while significantly reduced computational effort is needed, compared to a single grid methodology. The steady state methodology is also extended to transient conditions. Brief description of these methodologies is presented below, with technical details developed in the subsequent chapters.

The steady state multi-scale method utilizes compact modeling at component/module level, and reduced order modeling at subsystem/system levels. First, a compact model is developed for each component. These compact models represent the component/module at subsystem level simulations. Secondly, the cabinet is decomposed into multiple subsystems such as enclosures and plena, and a reduced order model (ROM) is developed for each subsystem with the replaced compact models for the components and modules. Thirdly, all ROMs are interconnected together through an efficient interfacial-coupling scheme based on the concept of flow network modeling (FNM) to simulate the entire cabinet. The heat and mass flow rates and static pressure at each interface are coupled through this scheme. The full-field solutions for compact components, subsystems and the entire system are therefore available.

In order to achieve a detailed solution at the component level, a 'zoom-in' approach is utilized. First, thermal information from the system level simulation, in terms of component surface temperatures, local heat transfer coefficients and reference temperatures, or heat fluxes, are extracted. Secondly, these quantities are interpolated on a finer grid and further employed in component level thermal analyses as boundary conditions. The locally zoomed in component/module models utilize the heat conduction equation on a fine grid, employing solutions from previous steps. At this stage, components are modeled in greater detail, capturing such features as the chip, lead frame, and die attach. Thus, thermal analyses at different levels are bridged, with good accuracy and significant saving in computational time.

A boundary capturing scheme is introduced to the multiscale modeling approach, significantly broadening its applications. The output of the subsystem upstream is used as the input to the adjacent subsystem downstream during the system observation generation process of reduced order modeling. A flow straightening duct is usually necessary to be added to the subsystem model upstream to better approximate the boundary profile of the air flow. The integrated heat and mass fluxes, and the average pressure, instead of the boundary profiles, are coupled at each interface by assuming there is a unique map between the profile and its integral.

The transient multi-scale thermal modeling methodology applies compact modeling at component and module levels, and reduced order modeling at enclosure level. A general approach to develop the multi-layer dynamic compact models for components and modules is described.

The proposed steady-state multi-scale thermal analysis approaches are implemented for a thermoelectrically cooled cabinet, a simulated server rack, and a test vehicle with double-sided cooling. The transient multi-scale thermal modeling approach was examined for an electronic enclosure containing one IGBT module with four IGBT devices, and a single enclosure of the test vehicle with double-sided cooling. The simulation results under both steady state and transient scenarios are in good agreement with experimental measurements.

The flow chart in Figure 1.7 presents the research activities carried out as part of this dissertation.

Chapter 2 introduces compact modeling and reduced order modeling. The mathematical formula for the POD reduced order modeling is described, and the multiscale analysis framework for a thermoelectrically cooled cabinet is presented.

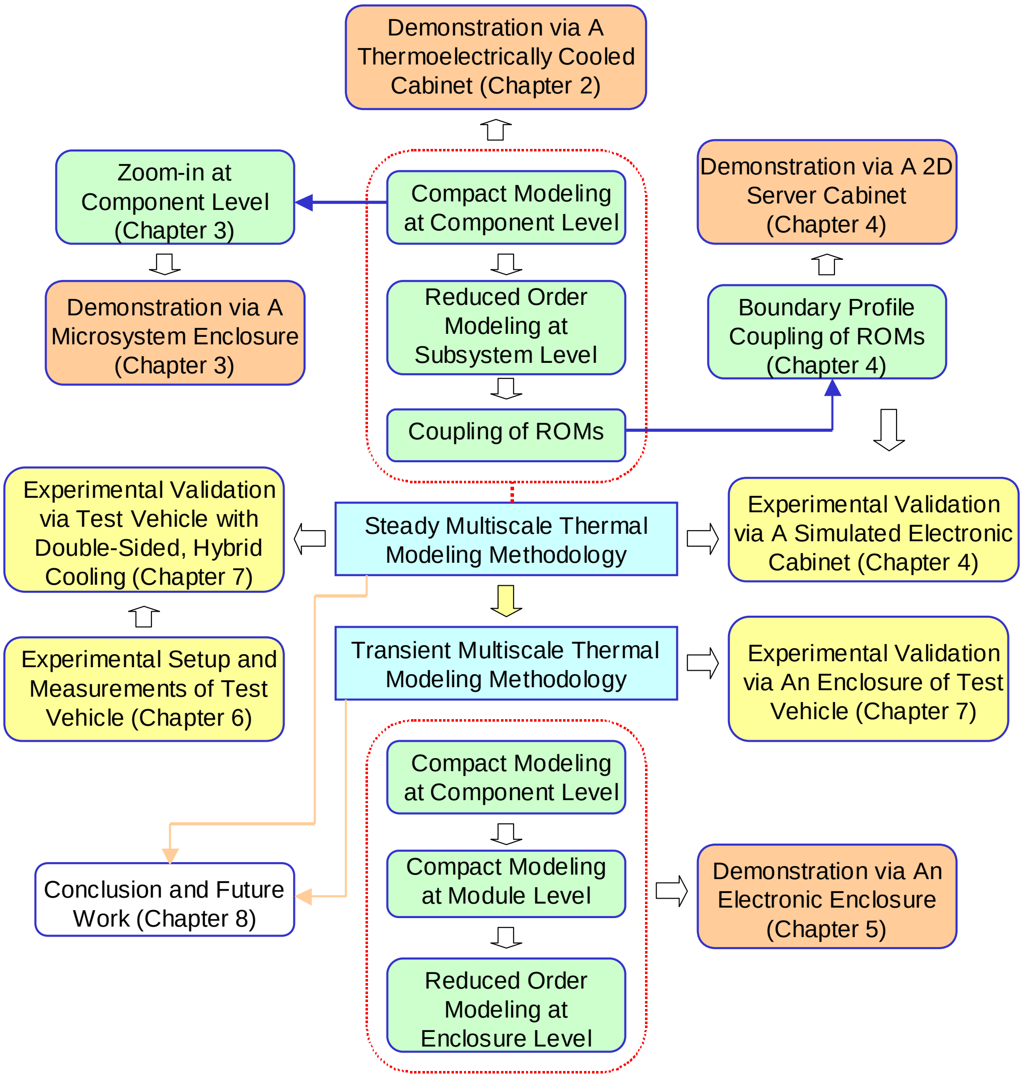



Figure 1.7 Flow chart of current work

Chapter 3 describes zoom-in approach based multi-scale modeling for a microsystem enclosure. Detailed simulations at component and system levels are achieved.

Chapter 4 illustrates multi-scale thermal modeling with boundary profile capturing capability, and the simulations results are supported by measurements conducted on simulated server cabinet.

Chapter 5 describes transient multi-scale thermal modeling methodology, illustrated through application to an electronic enclosure with an IGBT module containing four IGBT devices. A general approach to develop dynamic compact models for the components and module is presented.

Chapter 6 illustrates the design and construction of a test vehicle with double-sided hybrid cooling and experiments. The effects of system variables on the thermal performance of the cabinet are investigated.

Chapter 7 describes the multi-scale thermal modeling of the test vehicle with double-sided hybrid cooling. Compact models are developed for various components inside the system, and reduced order models are developed for the subsystems. The modeling results are validated through measurements.

Chapter 8 provides the conclusion and future work of this dissertation.

## 1.4 Literature Review

The following review focuses on the modeling strategies for the thermal and fluid flow analysis of electronic cabinet.

### 1.4.1 CFD/HT Modeling

CFD/HT modeling of electronic cabinets was introduced in 1985 by Latrobe et al. [8], who performed three-dimensional (3D) simulations on the predictions of the flow in cabinets containing parallel circuit board sets. Agreement to within 5% was found with laser Doppler anemometry (LDA) derived flow rates. Cadre and Viault [9] extended this work, comparing predictions with temperature rise measurements. Sloping surfaces were modeled using disjointed lines and agreement to within 3 °C was found.

Kobayashi *et al.* [10] developed a compact model for each terminal of a closed cabinet by using empirical correlations to model the pressure drop in each terminal (board channel). Experiments were conducted to get the temperature efficiency which represents the heat rejection effect of the heat exchanger inside the cabinet. A simplified model of the heat transfer through the heat exchanger was developed. The entire system was simulated through CFD/HT by utilizing the compact models for each terminal and heat exchanger.

Ogushi and Yamanaka [11] used flow network modeling based on empirical correlations to get the flow distribution within the cabinet and then applied the CFD/HT modeling to a single channel inside the cabinet to study natural convection. An improved combination of flow network modeling and CFD simulation is present by Kowalski and Redmehr [12]. First, the CFD simulations were conducted for each individual card passage to get the pressure drop and effective heat transfer coefficients through each passage. Secondly, the flow network modeling with SIMPLE algorithm was conducted utilizing the pressure drop correlations and effective heat transfer coefficients obtained by the CFD simulation for each passage. Finally, CFD simulation was conducted again for each card passage with detailed components mounted to the board. The predicted flow rates through each card passage are within 10% of experiments.

Wei [14] studied the thermal and airflow characteristics within a server cabinet using a Virtual Product Simulator (VPS)/simulation hub developed by Fujitsu. The original CFD/HT model of the server cabinet contains more than 1.5 million grid cells, which were reduced to below 1 million by deleting unimportant components.

Extensive efforts have been focused on enclosure level simulation. Wankhede *et al.* [19] investigated the effect of the solar heating loads on the thermal performance of an outdoor air sealed enclosure. Various cooling techniques were studied through CFD/HT modeling. It was found that using air-to-air heat exchanger is the most effective solution for cooling the enclosure. Linton and Agonafer [20] performed system level thermal modeling of an IBM PC by using the commercial software PHOENICS. They modeled totally 28 components represented as rectangular blocks. As high as 23% difference between measured and calculated component temperatures was reported. Lasance and Joshi [21] summarized the status and challenges of numerical modeling on natural convection in electronic enclosures.

### 1.4.2 Reduced Order Modeling

(1) Reduced order modeling taxonomy

To address the difficulties associated with system level numerical modeling, efficient solution procedures have been explored. Among these, reduced or compact models have gained some popularity for thermal analysis of electronic systems [25-27]. Shapiro [28] presents a historical review of the reduced order modeling of complex electronic systems.

The process of *model reduction* is to transfer a model of a large number of DOF, either from numerical simulations or full-field experimental measurements, to a model of significantly fewer DOF. The numerical model after model reduction is termed as reduced order model (ROM). Figure 1.8 illustrates this taxonomy of reduced order modeling [28].

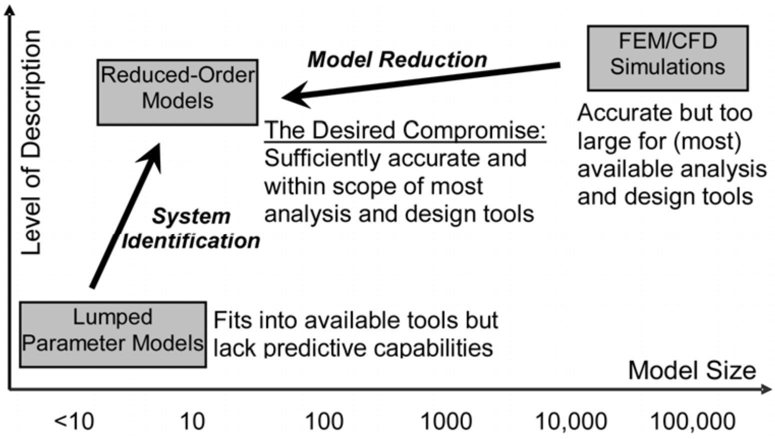



Figure 1.8 Model description and size comparison [28]

(2) Classification of reduced order modeling

The method of reduced order modeling is divided into state space modeling and distributed parameter system modeling by Rambo [29]. State space methods reduce a system to a 'black box' with input and output, which is also synonymous with 'lumped-parameter model'. Distributed-parameter modeling aims to approximate the physics over the entire domain, as opposed to returning a vector of desired outputs. Since the models created by state space modeling and the models of component or modules created by distributed-parameter system approach are typically called compact models, the reduced order modeling is divided into compact modeling and reduced order modeling here. The compact modeling approach are typically used for the linear solution of components and modules, while the reduced order modeling is widely used for creating low order models of nonlinear problems such as fluid flow and heat transfer.

(3) Compact modeling

Use of suitable compact component models in system level analysis has been considered to reduce the disparity in length scales involved and therefore the mesh size and solution time of the numerical model. A compact thermal model of a component has reduced complexity in representation and thermal properties, but provides relatively accurate description of the thermal behavior of the component within a system environment [27]. Linton and Agonafer [22] developed a coarse finned heat sink model that can be used in system models. As few as 3x4x3 cells were used to represent a finned heat sink. An approximation error of 18% was reported with the coarse numerical model, compared to the experimental data and the detailed model. Narasimhan and Bar-Cohen [30, 31] improved the modeling accuracy of the heat sink using a porous medium model. Agreements between the detailed model and the porous medium model were reported within 11% and 17.2% for pressure drop and base temperature predictions, respectively.

Lasance et al. [26] presented an approach to develop boundary condition independent compact models based on optimization. Detailed CFD/HT simulations were conducted for a 208-PQFP validation chip under a total of 200 boundary conditions. A thermal resistance network with 7 thermal resistors was constructed for the validation chip. The predicted junction temperature rise using the thermal resistance network based compact model was reported within 3.1% for various boundary conditions, compared to the detailed numerical modeling results. An electro-thermal model for thermoelectric modules (TEC) was developed by Chimchavee et al. [32]. Thermal resistance network was constructed for the TEC module and solved by PSPICE. The simulation results were reported equal to the calculation results using the lumped system model.

Bagnoli et al. [33] present a transient thermal resistance analysis for power electronic devices by induced transient method. A thermal circuit analogous to electric RC circuit was created and solved in frequency domain by transferring the junction temperature rise from time domain to frequency domain through Laplace transformation. This method was applied to a simulated 1-D structure, but no modeling error was reported. Luo [34] created a dynamic compact model for the insulated gate bipolar (IGBT) module by using the measurements. The experimental transient thermal impedance was fitted into a series that consists of a finite number of exponential terms, and a thermal circuit was created based on these terms. A modeling error of 11% was reported for the prediction of transient thermal impedance, compared to detailed numerical simulation with Ansys. Experimental measurements were also used by Rencz et al. [35] to develop boundary condition independent dynamic compact models of packages and heat sinks. Selected boundary conditions from the sets used by Delphi Project were applied to the packages and a dynamic thermal circuit was constructed using optimization analysis.

Hocine et al. [36] modeled the thermal effects in high power IGBTs using three-dimensional transmission line matrix (TLM) simulation method. This approach approximated the heat diffusion equations with transmission line network equations by neglecting the inductance term. A transient thermal resistance network was constructed based on the transmission line network, but no modeling error was reported. Habra et al. [37] conducted the thermal analysis of the multi-chip package using the dynamic compact thermal modeling. A separate transient thermal circuit was created for each chip and the junction temperatures were obtained through superposition method. An approximation error of 2% for the junction temperature instead of the temperature rise was reported compared to the COMSOL simulations.

(4) Reduced order modeling

The fundamental principle of reduced order modeling is to find a suitable set of modes to characterize the solution space of the system, and the governing equations of the system are projected onto these modes, reducing the solution procedure to finding the appropriate weight coefficients that combine the modes into the desired approximate solution. Traditional modal expansions form the basis in frequency domain with spectral methods using Fourier series or orthogonal polynomials (Legendre, Chebyshev, Laguerre). The spectral methods are limited to systems of relative simple geometry and boundary conditions. The types of boundary conditions often dictate the functions employed in the expansion in spectral methods. For example, Chebyshev polynomials are often exploited for inhomogeneous boundary conditions while Fourier series are the natural choice for periodic domains. Typically, many terms (modes) are needed for accurate predictions of the system response, especially, higher order terms are required to resolve sharp gradients in the solution.

The proper orthogonal decomposition (POD) assembles the model-specific optimal linear subspace from an ensemble of system observations. Owing to its stochastic nature in the subspace calculations, the POD is ideally suited for nonlinear phenomena and has been used extensively in low-dimensional modeling of turbulent flows [38] and laminar flows [39-44].

The existing POD methodology to date is limited to problems with a small range of modal parameters. A large number of system observations is typically needed. Holmes et al. [38] investigated the dynamics of a prototypical system under a single Reynolds or Rayleigh number or limited range of variation. Deane et al. [39] studied the laminar flows with 52 observations over a small range of Reynolds numbers. Ma and Karniadakis [40] used 40 modes to study the limit cycle of three-dimensional transitional flow around a cylinder at a critical $Re$ =188 and at $Re$ = 610. Rowley et al. [41] modeled the compressible flows within a cavity under a Mach number of 0.6 using 51 snapshots. An approximate isentropic version of the Navier-Stokes equations was used to reduce the complexity associated with the Galerkin projections.

In reduced order modeling of heat transfer, Park and Cho [42] partitioned the linear governing equations into homogeneous and inhomogeneous components, which satisfy the homogeneous boundary conditions and inhomogeneous boundary conditions, respectively. A set of 200 and 400 observations were generated to solve the temperature and species transport within a square domain with a quarter removed, respectively. Sirovich [43, 44] studied the dynamics of natural convection using around 200 observations. Park and Li [45] studied Rayleigh-Bénard natural convection within a rectangular cavity with reduced order modeling. A set of 30 sinusoidal boundary heat flux profiles for a total of 3,000 observations were used to create the reduced order model of the controller that controls the intensity of Rayleigh-Bénard convection.

One key concern in the existing POD methodology is determining the weighted coefficients for the POD modes. In the past, Galerkin projection method was typically used by projecting the governing equations onto the subspace spanned by the POD modes [38-51]. One major limitation of the traditional method is that it is only applicable to configurations with homogeneous boundary conditions. To solve inhomogeneous problems, both Park and Kim [47] and Ravindran [46, 50] suggest homogenizing the POD modes by subtracting a reference field that satisfies the governing equations. The homogenization of POD modes may eliminate the need for boundary pressure-velocity coupling during Galaerkine Projection process. Park and Kim [47] constructed a low-dimensional controller for flow over a backward facing step using 1,000 observations with two inlet velocity profiles. Ravindran [46, 50] generated 100 homogenized observations to develop a reduced order flow controller using blowing at $Re = 200$.

The Galerkin projection may produce false limit cycles [49] and ultimately yield unphysical results by de-emphasizing important modal contributions under varying bifurcation parameters in parameter dependent flows [48, 51]. Also the homogenization of POD modes described above may require full numerical computations for each new set of boundary conditions.

To avoid the expensive homogenization procedures, Ly and Tran [52] proposed a simple approximation method based on interpolating splines between weight coefficients of POD modes to match a desired parameter value. They studied the steady state Rayleigh-Bénard natural convection within a square domain by interpolating the weight coefficients of POD modes under different Rayleigh numbers. Galletti *et al.* [[53] modeled transient laminar flow over a confined square block by interpolating the modal weight coefficients at different Reynolds number to correct the pressure drop across the duct from 160 observations. This method would require higher order multi-dimensional interpolation to model a complex system with multiple parameters and also does not guarantee that the desired parameter level will be achieved. A flux matching approach was proposed by Rambo [13, 54], which enforces the POD modes to satisfy the flux or its integral condition such as mass or heat flow rate at the boundaries. This technique overcomes the limits of both Gerlerkin projection method and coefficients interpolation method, but fixed or uniform input boundary conditions are needed for the flux matching at the boundaries.

# CHAPTER 2

# MULTISCALE THERMAL MODELING METHODOLOGY OF ELECTRONIC CABINET

Fluid and thermal transport processes occur across multiple length scales in thermal management of electronic systems [6, 29]. Characterization and modeling of these multi-scale systems are challenging and often impractical because each system may contain a variety of different subsystems and each subsystem may contain different electronic components. The number of degrees of freedoms (DOF) of such a system may be too large to be resolved by existing computational techniques and hardware. One strategy to bridge length scales is to develop separate models for individual components and assemble them to model the complete system [55, 56]. Various levels of description for different components can be achieved. Modularization of individual subsystem models affords the ability to quickly integrate components into a new system model, without developing a new computational grid for altering the subcomponent models.

## 2.1 Framework of Multiscale Thermal Modeling Methodology

Many electronics systems such as electronics cabinets are modular in nature, consisting of a series of nested sub-domains. The general approach here is to divide such a system into multiple sub-domains or subsystems. Each sub-system may also comprise of multiple components. Therefore, at least three levels need to be addressed: system level, subsystem level, and component level. The framework of the multiscale thermal modeling at these three levels is shown in Figure 2.1 [15, 56, 57]. At first, a compact model (CM) is developed for each component and is used to replace the detained component model inside the subsystem. Secondly, a reduced-order model (ROM) with input and output information is constructed for each subsystem separately. Finally, the ROM for each subsystem is subsequently linked together to model the complete system. This framework can be extended to include more length scales, such as module level and data center level. The concepts of compact modeling and POD reduced order modeling will be discussed in the following sections. This multiscale thermal modeling methodology will be demonstrated through an example in this chapter.

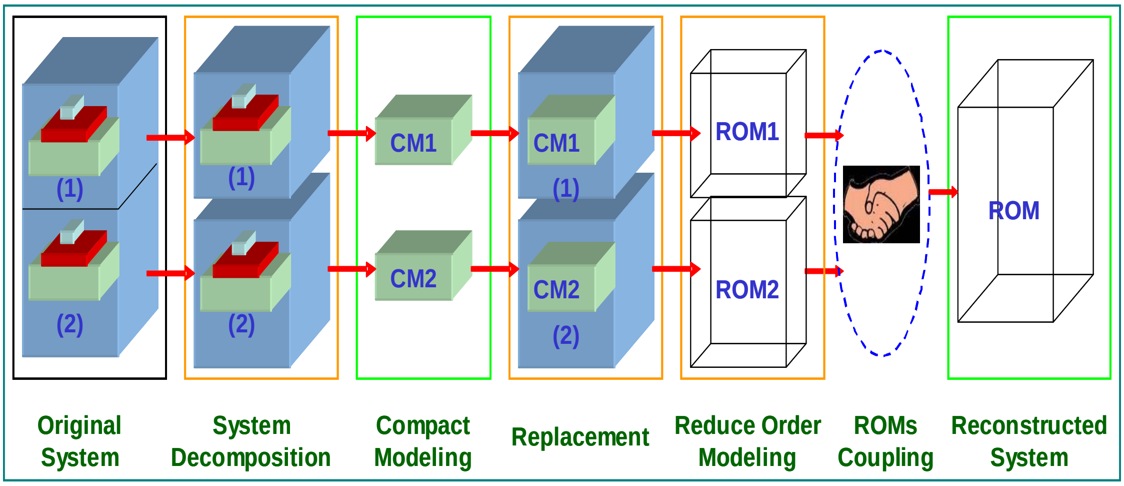
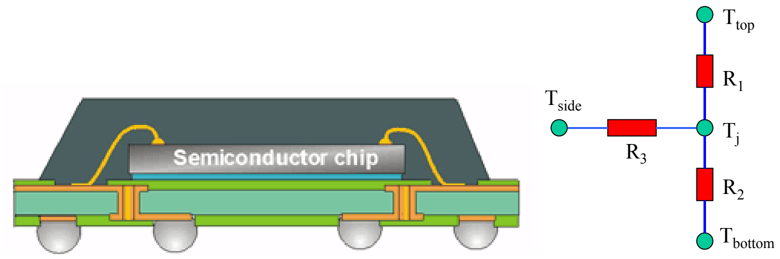



Figure 2.1 Framework of multiscale thermal modeling methodology

## 2.2 Compact Modeling

Compact modeling has been intensively studied at device level [58-62]. This class of modeling is also synonymous with 'lumped-parameter modeling' or 'state-space modeling' and can utilize basic physical principles such as mass and energy conservation as well as correlations to develop the model behavior [29]. As the most popular approach of the compact modeling, resistance network modeling (analogous to electrical resistance network modeling) has been widely used to study the device junction temperature under different boundary conditions [59-62]. Figure 2.2(a) shows the schematic of a BGA package, and Figure 2.2(b) depicts a simple thermal resistance network with three thermal resistors. Given certain boundary conditions such as external heat transfer or ambient temperature, the temperature at the junction or surfaces of the chip can be obtained by solving this thermal resistance network.

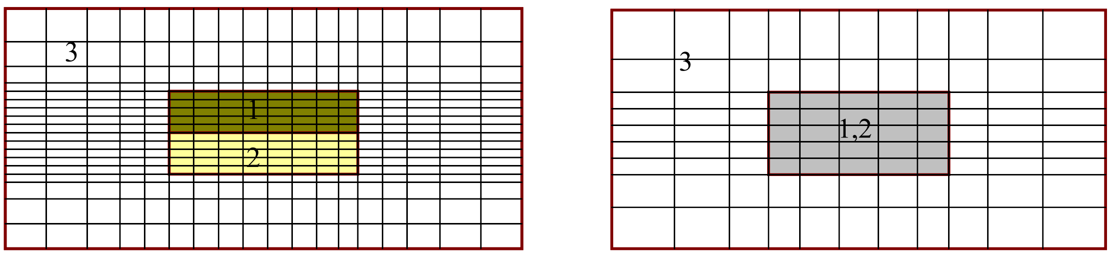



(a) ( b)

Figure 2.2 BGA package, (a) schematic view, (b) thermal resistance network

Although thermal resistance network modeling is easy to solve and yields acceptable prediction of the chip junction temperature, it is difficult to incorporate into system level simulation. Most current thermal resistance network modeling is to impose a number of boundary conditions on the package and conduct detailed numerical modeling or experiments to construct the thermal resistance network for the package. Although a boundary conditions independent (BCI) thermal resistance network model can be achieved through this approach, it is only appropriate for post-processing. It is impossible to remove the detailed package model at the system level simulation without changing the system model through thermal resistance network modeling. Another major disadvantage of thermal resistance network modeling is that the description of the underlying physical mechanisms is very incomplete. Only certain thermal information such as chip junction temperature can be obtained.

Multi-layer compact modeling is another compact modeling approach, which can be incorporated into system level simulation [15, 27]. In conventional discretization schemes, the smaller package length scales result in a larger number of control volumes in the surrounding fluid regions where fewer volumes might suffice. This is because the discretization required in the package translates into the fluid regions, and vice versa. Multi-layer compact modeling attempts to eliminate the small length scales associated with modeling the details of the package by using models with length scales comparable to those required by the system level CFD simulation. The idea of the compact modeling can be seen from the example shown in Figure 2.3(a), where a large domain (e.g. an electronic enclosure) contains two smaller blocks (e.g. a package with two layers). A typical hexagonal mesh will result in about 324 nodes for this model. If these two blocks can be merged together through some approach, as shown in Figure 2.3(b), a typical hexagonal mesh will only result in about 99 nodes, with a reduction of 70%. Since the simulation time of CFD modeling is proportional to the computational nodes of the numerical model, much computational cost can be save through the model shown in Figure 2.3(b).




(a) (b)

Figure 2.3 Multi-layer compact modeling, (a) detailed model, (b) compact model

Since the multi-layer compact model of the package can be still remained in the system model, it is very convenient to be incorporated into the system level simulation without changing the system model. However, multi-layer compact model is more difficult to construct, compared to the thermal resistance network model. It is also more complex than the thermal resistance network model, which means less computational cost can be save at the component level simulation. The most challenging part of the multi-layer compact modeling is how to find out which layers or materials can be merged together, and how to find out the thermal properties of the newly formed layers. This will be described through several examples in this thesis for both steady state and transient multi-layer compact modeling.

## 2.3 Reduced Order Modeling

Although reduced order modeling can be also used at the component level simulation [63-65], especially solving transient nonlinear problem associated with the thermal-mechanical analysis of the package [66], it is more often used at the system level simulation [13, 67, 68], due to its capability to significantly reduce the degrees of the freedom of the system model.

### 2.3.1 Reduced Order Modeling Taxonomy

The reduced order modeling also refers to distributed parameter system approach [29]. It aims to approximate the physics over the entire domain, as opposed to returning a vector of desired outputs. As we know, for the numerical modeling with finite difference method (FDM), the partial differential equation (PDE) at each node is transferred into a matrix of the nodal variables by finite difference equation. While for the numerical modeling with finite element method (FEM), the PDE at each element is approximated by ordinary differential equation (ODE). The fundamental principle of reduced order modeling is to reduce the number of ODE (FEM) or PDE (FDM) associated with the detailed numerical model of the system into a smaller number of ODEs to be solved, as shown in Figure 2.4. The reduction of the ODEs can be achieved by finding a suitable set of modes to characterize the system space to project the governing equations onto, reducing the solution procedure to finding the appropriate weight coefficients that combine the modes into the desired approximate solution.

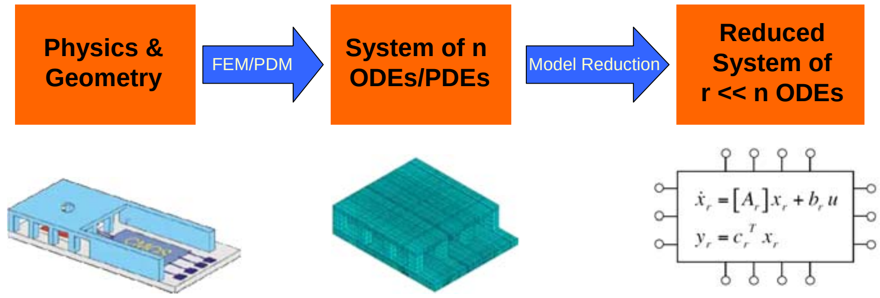



Figure 2.4 Reduced order modeling taxonomy

Traditional modal expansions using Fourier series or orthogonal polynomials (Legendre, Chebyshev, Laguerre) form the basis for spectral methods. Complex boundary conditions can be problematic in spectral methods and the types of boundary conditions often dictate the functions employed in the expansion. For example, Fourier series are the natural choice for periodic domains while the properties of Chebyshev polynomials are often exploited for inhomogeneous boundary conditions [29]. Higher order terms are required to resolve sharp gradients in the solution and many terms in the series are needed for accurate predictions.

### 2.3.2 The proper orthogonal decomposition (POD)

We begin by giving an overview of the POD framework for reduced-order modeling in this section. Consider a three-dimensional steady incompressible turbulent flow with negligible buoyancy effects. The Reynolds Averaged Navier-Stokes (RANS) continuity, momentum and energy equations are

$$\nabla \cdot \mathbf{u} = 0 \tag{2.1a}$$

$$\mathbf{u} \cdot \nabla \mathbf{u} - \nabla \cdot (\nu_{eff} \nabla \mathbf{u}) + \frac{1}{\rho} \nabla P = 0 \quad (2.1b)$$

$$\rho c_p \mathbf{u} \cdot \nabla T - \nabla \cdot (\kappa_{eff} \nabla T) = 0 \quad (2.1c)$$

where $\nu_{eff} = \nu + c_\mu \frac{k^2}{\varepsilon}$ and $\kappa_{eff} = \kappa + \frac{c_p \nu_t}{\rho Pr_t}$ with $Pr_t = 0.85$ and can be computed through any RANS-based turbulence model and non-equilibrium wall functions [69]. For now, assume we have a reduced-basis of dimension $n$, $\{\varphi_i(\cdot)\}_{i=1}^n$ with $\varphi_i(\cdot) \in H^2(\Omega)$. With this basis, the reduced-order approximation to the velocity vector $\mathbf{u}$ is represented as

$$\mathbf{u}^r = \sum_{i=1}^r a_i \varphi_i, r \le n \quad (2.2)$$

where the modes $\varphi_i(x)$ can be obtained through the method of snapshots [70]:

$$\varphi_i = \sum_{j=1}^n \gamma_{i,j} \mathbf{u}_j \quad (2.3)$$

and the weight coefficients matrix $\{\gamma_{i,j}\}_{i,j=1}^n$ here are eigenvectors of the solution to

$$D\varphi(x) = \lambda \varphi \quad (2.4)$$

where $D = \mathbf{U}^T \mathbf{U} / n \in R^{n \times n}$ with $\mathbf{U} = \{\mathbf{u}_1, \mathbf{u}_2, ..., \mathbf{u}_n\} \in R^{m \times n}$. The coefficients $a_k$ in Equation (2.2) are typically solved by Galerkin projection method, which projects the governing equations (1a) – (1b) into the space spanned by the POD modes $\varphi_k(x)$

$$(\nabla \cdot \mathbf{u}^r, \varphi_i) = 0 \quad (2.5)$$

$$(\mathbf{u}^r \cdot \nabla \mathbf{u}^r, \varphi_i) - (\nabla \cdot (\nu_{eff} \nabla \mathbf{u}^r), \varphi_i) + \frac{1}{\rho}(\nabla P, \varphi_i) = 0 \quad (2.6)$$

However, homogenization of boundary conditions is required with this method to eliminate the need for velocity and pressure or temperature coupling at the boundaries. A flux function, usually given as an integral condition such as mass flow rate, is defined on the boundary [13, 54]

$$F_m(\mathbf{u}) = \int_{\Gamma_m} \rho \mathbf{u} \cdot \mathbf{n} dA,\ \Gamma_m \subseteq \Omega \tag{2.7}$$

The goal is to fit the POD modes to match a goal flux function $G_m = F_m(\mathbf{u}^r)$ corresponding to the reduced-order velocity vector by solving the following least squares problem

$$\min\{\| G_m - \sum_{i=1}^{r} a_i F_m(\varphi_i) \|\} \tag{2.8}$$

The weighted coefficient vector $\mathbf{a} = \{a_i\}_{i=1}^{r}$ here can be computed as

$$\mathbf{a} = F_m^{+}(\Phi) G_m(\mathbf{u}^r) \tag{2.9}$$

where $F^{+} = (F^T F)^{-1} F^T$ is the Moore-Penrose matrix pseudo-inverse producing the least squares approximation, and $\Phi = \{\varphi_1, \varphi_2, \cdots, \varphi_n\}$.

To alleviate the poor approximations for solutions far from the system reference point in parameter dependent flows, a weighted POD was proposed in [71] by preweighting certain modes to increase their contribution on the superposition. One concern with this method lies in the fact that weighting is not unique and additional information about which modes to weight is required. Furthermore, the POD subspace is collapsed to a point near that single observation or snapshot as its weighting factor increases. To solve these problems, a complimentary POD (PODc) or pre-defined POD (p-POD) was described in [54, 71], which decomposes the POD subspace into orthogonal complement subspaces:

$$\Phi = \varphi^{\perp} + \varphi', \text{ where } \varphi^{\perp} \in R^{n \times s} \text{ and } \varphi' \in R^{n \times r - s} \tag{2.10}$$

The orthogonal complement set $\varphi^{\perp}$ is chosen to best satisfy the inhomogeneous boundary conditions and $\varphi'$ describes the flow features over the rest of the POD domain. For instance, the two snapshots ($s$=2) whose boundary conditions are closest to the test boundary condition can be used to construct $\varphi^{\perp}$, and the rest of the snapshots for $\varphi'$. The modal expansion and minimization problem are modified to

$$\mathbf{u}^r = \mathbf{u_o} + \sum_{i=1}^{r} a_i \varphi_i, \varphi_i \in \Phi = \{\varphi^{\perp}, \varphi'\} \tag{2.11}$$

$$\min\{\| G_m - F_m(\mathbf{u_o}) - \sum_{i=1}^{r} a_i F_m(\varphi_i) \|\} \tag{2.12}$$

where $\mathbf{u_o}$ represents the source function for velocity.

The flux matching procedure (FMP) can be extended to include the energy equation. Accordingly the heat flux function can be defined analogous to (5) as

$$F_h(T) = \int_{\Gamma_h} \kappa \nabla T \cdot \mathbf{n} dA,\ \Gamma_h \subseteq \Omega \tag{2.13}$$

The heat flux control surfaces are typically defined at the 3 surfaces of each heating component or the inlet of a flow domain. Since temperature field depends on the velocity field, the temperature complementary POD subspace $\phi^{\perp}$ is constructed with the snapshot whose velocity boundary condition is closest to the test velocity boundary condition. Additionally, multiple snapshots closest to the test temperature boundary conditions are selected. Similarly, the temperature solution can be approximated by

$$T^r = T_o + \sum_{i=1}^{r} b_i \phi_i, \phi_i \in \Psi = \{\phi^{\perp}, \phi'\} \tag{2.14}$$

where $T_o$ is the temperature source term. The modal coefficients vector $\mathbf{b} = \{b_i\}_{i=1}^{r}$ in Equation (2.14) can be obtained by solving the following optimization problem

$$\min\{\| G_h - F_h(T_o) - \sum_{i=1}^{r} b_i F_h(\phi_i) \|\} \tag{2.15}$$

If the eigenvalues $\lambda_i$ of the covariance matrix $D$ defined in Equation (2.4) are sorted in decreasing order: $\lambda_1 > \lambda_2 > ... > \lambda_n$ , then the POD mode $\varphi_1(x)$ corresponding to the maximum eigenvalue $\lambda_1$ is the principal axis of the solution domain. It captures the most kinetic energy of system, and the rest of the modes are in decreasing order of the corresponding eigenvalues. Therefore, it is possible to use only the first several POD modes to reconstruct the solution domain

## 2.4 Model Problem

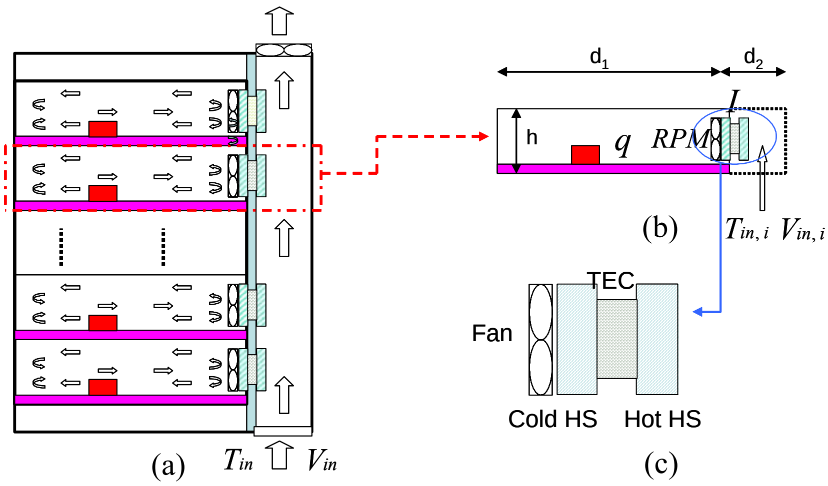



Figure 2.5 (a) cabinet, (b) single server enclosure and plenum, and (c) thermoelectric module (TEC) with two heat sinks (HS) and fan.

To illustrate the framework of multi-scale thermal modeling depicted in Figure 2.1, a three-dimensional representation of a typical data processing cabinet with multiple enclosures (each 2U or 0.0889m high) is considered, as shown in Figure 2.5. Cold air is delivered to the rack through the inlet at the bottom and is drawn across the heat sink attached to the hot side of the TEC. Within each enclosure, a single discrete heat source (component) is attached to a conducting substrate or printed wiring board. While the approach described is not limited to a single heat source, the model describes a common condition of a single dominant power dissipation component, such as a microprocessor package. A circulation fan is placed on the front of the heat sink attached to the cold side of TEC. Heat generated from the electronic component in each server enclosure is removed by circulation of cold air from the cold side of the TEC and is rejected from the hot side of the TEC to the flowing coolant stream. Heat sinks are provided on each side of the TEC for increased surface area. Illustrative enclosure and plenum dimensions are based on commercially available units. For this cabinet system, the inputs are the plenum inlet mean air velocity and temperature, the component heat generation rate, fan speed (RPM) and electrical current to the TEC. The outputs of interest are the temperature and flow field within each enclosure and plenum domain. Figure 2.5(b) describes a single enclosure and its associated plenum, which are collectively called enclosure subsystem here. Its representative geometry utilized in the illustrative simulations is shown in Table 2.1.

Table 2.1 Geometry of Enclosure and Plenum of Cabinet

| | | |
|---|---|---|
| Height ($h$) | 0.0889 | [m] |
| Length of Enclosure ($l_1$) | 0.512 | [m] |
| Length of Plenum ($l_2$) | 0.1 | [m] |
| Width of Enclosure ($w$) | 0.45 | [m] |

The multi-scale thermal modeling approach developed here involves sequential modeling at three different levels: component (TEC), enclosure subsystem, and cabinet. Specifically, a compact model for the TEC is first developed. A reduced order model (ROM) is then constructed via POD for the enclosure subsystem based on POD. The higher level ROM for the cabinet consisting of several such enclosure subsystems is obtained directly by stacking such enclosure subsystems, as shown in Figure 2.6.

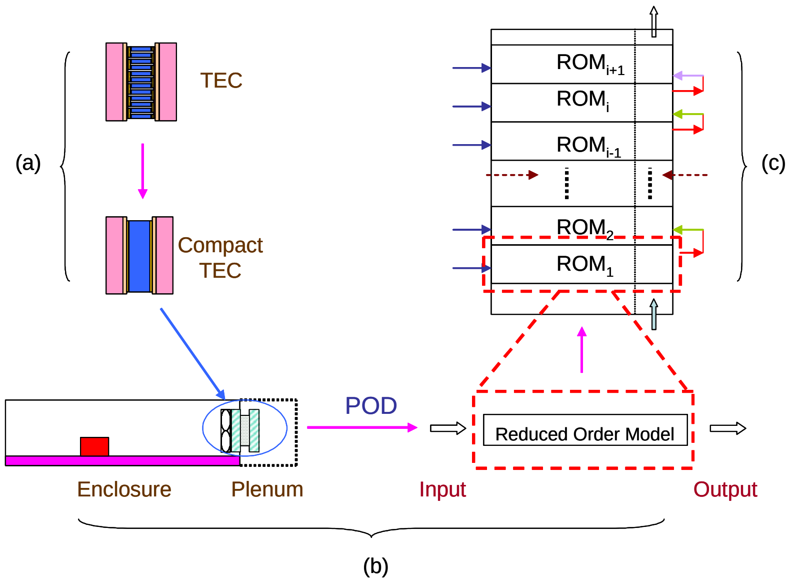



Figure 2.6 Multi-scale thermal modeling methodology: (a) component level, (b) enclosure level, and (c) cabinet level

## 2.5 Multi-layer Compact Model of TEC

The schematic views of a typical TEC are shown in Figures 2.7(a) and (b), respectively [72]. The detailed numerical model of the TEC is shown in Figure 2.7(c) with representative properties utilized in the illustrative simulations shown in Table 2.2. On the two ends of TEC are the ceramic supports, and the attached copper tabs are used to electrically connect the pellet couples. Solder is used to attach the pellets or thermo-elements to the tabs and attach the tabs to the ceramic supports. For this study, copper blocks are attached to the cold and hot sides of TEC, as shown in Figure 2.7(c). On the top surface of the copper block on the cold side, a uniform heat flux is assumed. A uniform convection heat transfer coefficient is assumed on the bottom surface of copper block on the hot side.

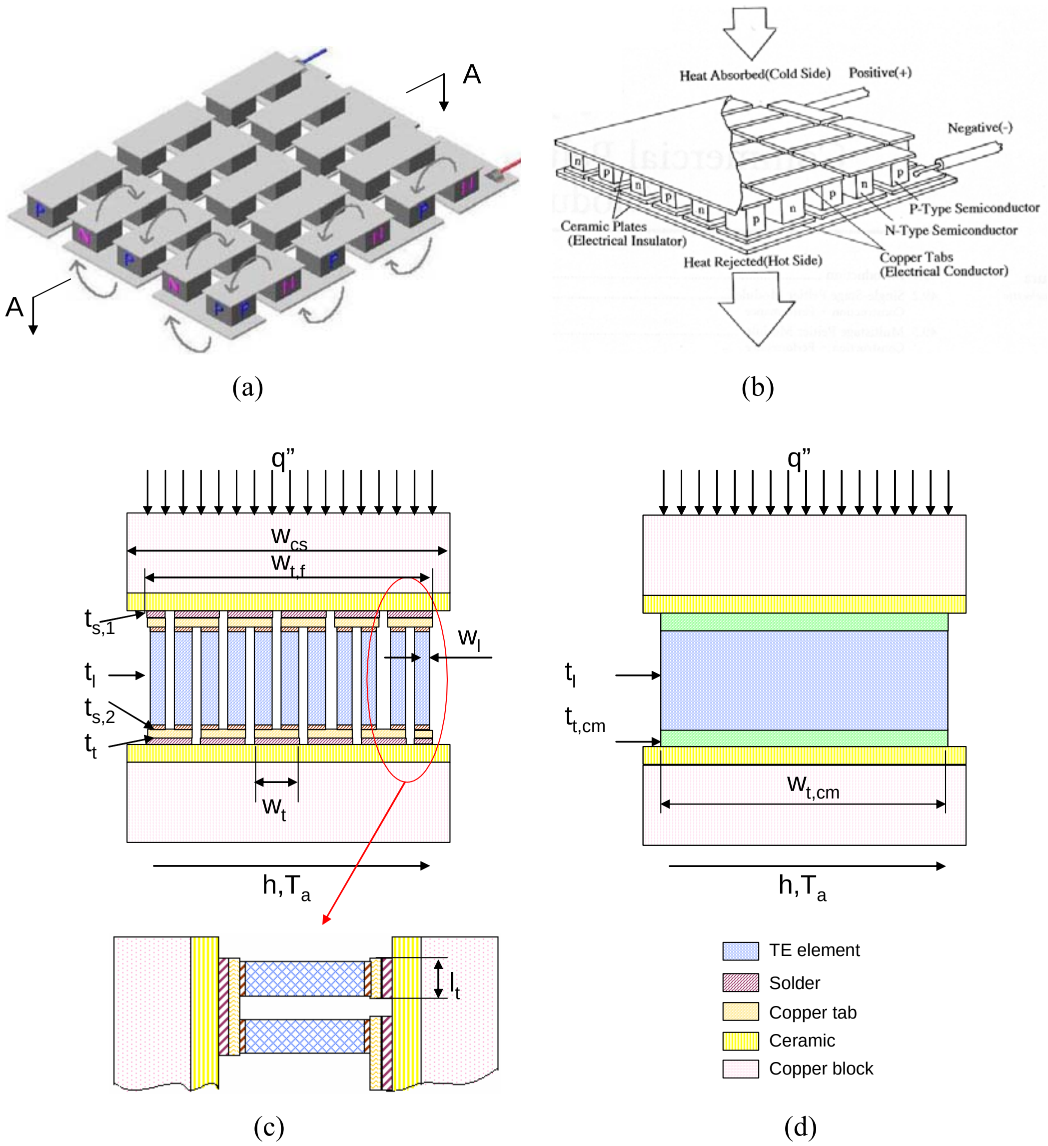



Figure 2.7 Thermoelectric cooler (TEC), (a) overall schematic, (b) electric current schematic [73], (c) detailed numerical model of TEC with two copper blocks, and (d) compact numerical model of TEC with two copper blocks.

For coupling with the flow domain, a compact multi-layer numerical model for the TEC is also developed, as shown in Figure 2.7(d). Five layers are included, including two ceramic support layers, two tab layers, and one thermoelectric (TE) leg layer. The two solder layers are included in the tab layer. The thicknesses of ceramic and TE leg layers remain the same as in the detailed model, and thickness of tab layer is the sum of tab and two solder layers in the detailed model in Figure 2.4(c).

Table 2.2 Specifications of TEC

| | | |
|---|---|---|
| $I_{max}$ (declared by manufacturer) | 8.5 | [A] |
| $Q_{c\ max}$ (declared by manufacturer) | 72.0 | [W] |
| $\Delta T_{max}$ (declared by manufacturer) | 65 | [°C] |
| Ceramic support thickness ($t_{cs}$) | 0.7 | [mm] |
| Ceramic supports width and length ($w_{cs}$) | 40 | [mm] |
| Ceramic thermal conductivity ($\kappa_{cs}$) | 39.7 | [W/m-K] |
| Solder (copper-pellet) thickness ($t_{s,1}$, $t_{s,2}$) | ~0.05 | [mm] |
| Solder thermal conductivity ($\kappa_s$) | ~19.1 | [W/m-K] |
| Copper-tabs thickness ($t_t$) | 0.3 | [mm] |
| Copper-tabs width ($w_t$) | 3.6 | [mm] |
| Copper-tabs full width ($w_{t,f}$) | 39.4 | [mm] |
| Copper-tabs length ($l_t$) | 1.4 | [mm] |
| TE leg thickness ($t_l$) | 1.1 | [mm] |
| TE leg width ($w_l$) | 1.2 | [mm] |
| Copper-tabs thermal conductivity ($\kappa_t$) | 387.6 | [W/m-K] |
| Number of thermoelectric couples ($N_{te}$) | 127 | [#] |
| TE Seebeck coefficient ($\alpha$) | $2.02\times10^{-4}$ | [Volts/K] |
| TE element thermal conductivity ($\kappa_l$) | $1.51\times10^{-2}$ | [W/m-K] |
| TE electrical resistivity ($\rho_l$) | $1.01\times10^{-3}$ | [$\Omega cm$] |

The effective thermal conductivities of the TE leg and tab layers in the compact model are given by Equations (2.16) - (2.19). The derivation is based on the compact model and detailed model having the same thermal resistance (see Appendix A for details).

$$\kappa_{t,cm}^{\perp} = \left(\frac{t_{s,1}}{\kappa_s N_{te} w_t l_t} + \frac{t_t}{\kappa_t N_{te} w_t l_t} + \frac{t_{s,2}}{2\kappa_s N_{te} w_l^2}\right)^{-1} (t_{s,1} + t_t + t_{s,2}) / w_{t,f}^2 \tag{2.16}$$

$$\kappa_{l,cm}^{\perp} = \frac{2\kappa_l N_{te} w_l^2}{w_{t,f}^2} \tag{2.17}$$

$$\begin{aligned}\kappa_{t,cm}^{//} = \{&\left(\frac{2l_t}{\kappa_s w_t t_{s,1}} + \frac{(w_{t,f}/\sqrt{(N_{te}+1)/2} - 2l_t)}{\kappa_a w_t t_{s,1}}\right)^{-1} + \left(\frac{2l_t}{\kappa_s w_t t_t} + \frac{(w_{t,f}/\sqrt{(N_{te}+1)/2} - 2l_t)}{\kappa_a w_t t_t}\right)^{-1} \\ &+ \left(\frac{1}{\kappa_s t_{s,2}} + \frac{(w_{t,f}/(2\sqrt{(N_{te}+1)/2}) - w_l)}{\kappa_a w_t t_{s,2}}\right)^{-1}\}/(t_{s,1} + t_t + t_{s,2})\end{aligned} \tag{2.18}$$

$$\kappa_{l,cm}^{//} = \left(\frac{1}{\kappa_l t_l} + \frac{\left(\frac{w_{t,f}}{2\sqrt{(N_{te}+1)/2}} - w_l\right)}{\kappa_a w_l t_l}\right)^{-1} / t_l \tag{2.19}$$

To take into account the Thomson and Peltier effects of TEC, energy source terms are added at the interfaces between the leg layer and tab layer on the cold and hot sides of the TEC. The energy source terms are evaluated at each iteration of the CFD/HT solution, and are used to couple the CFD domains representing the hot and cold sides of the TEC. The energy source terms for the cold and hot sides are described as

$$\Phi_{-,j} = -2N_{te}\alpha IT_{c,j} / A_c \quad \text{and} \quad \Phi_{+,j} = 2N_{te}\alpha IT_{h,j} / A_h \tag{2.20}$$

respectively, where $j$ is the index of nodes at the interface for the energy source term.

The TEC was investigated under steady state for two different current loads, 40% and 60% of the maximum current ($I_{max}$). A comparison between predictions using the compact model and the detailed model is presented in Table 2.3, which shows an error of less than 1%. Therefore, the multi-layer compact model for the TEC is considered sufficiently accurate for the enclosure level simulation.

Table 2.3 Simulation comparisons of two models

| I | Model | $Q_h$ (W) | $\overline{T}_c$ (K) | $\overline{T}_h$ (K) | $T_{max}$(K) |
|---|---|---|---|---|---|
| $0.4I_{max}$ | Compact | 42.5 | 292.3 | 328.2 | 328.4 |
| | Detailed | 42.6 | 291.9 | 328.3 | 328.5 |
| $0.6I_{max}$ | Compact | 74.9 | 292.1 | 349.7 | 350 |
| | Detailed | 75.0 | 291.6 | 349.9 | 350.1 |

### 2.6 Reduced Order Modeling For Electronic Enclosure

The POD method with flux matching technique is used in this work to construct the compact model for the enclosure subsystem shown in Figure 2.6(b). The flow fields inside the enclosure and within the associated plenum are considered independently, and solved separately. However, the temperature fields are coupled together and also depend on the flow field. Therefore, they need to be solved simultaneously.

For the flow within the plenum domain, a mass flux function is introduced at the plenum inlet and is matched by the POD modes. Similarly, a mass flux function is defined on the fan surface for the flow inside the enclosure. For the temperature fields inside the enclosure and plenum, two heat flow rate functions are defined as

$$F_{h_e}(T) = \int_{\Gamma_{h_e}} -\kappa \frac{dT}{d\mathbf{n}} \mathbf{n} dA,\ \Gamma_{h_e} \subseteq \Omega \tag{2.21}$$

$$F_{h_p}(T) = \int_{\Gamma_{h_p}} -\rho c_p \mathbf{u} T \mathbf{n} dA,\ \Gamma_{h_p} \subseteq \Omega \tag{2.22}$$

at the chip surface and plenum inlet surface, respectively. The temperature modes $\phi_k$ need to be fitted to match the goal function $G_h(T^r) = [G_{h_e}, G_{h_p}]' = [F_{h_e}(T_e^r), F_{h_p}(T_p^r)]'$ corresponding to the desired enclosure and plenum temperature fields. The weighted coefficients vector $\mathbf{b} = \{b_i\}_{i=1}^{r}$ for the temperature modes are therefore given by

$$\mathbf{b} = F_h^{+}(\phi) G_h(T^r) \tag{2.23}$$

To justify the accuracy of POD results, the following Euclidean *L2* error norm is defined

$$V_{err}^{r} = \frac{\| V^r - V^t \|}{\| V^t \|} \tag{2.24}$$

where $V$ represents velocity and temperature rise over ambient temperature, respectively.

The observations for the enclosure and its associated plenum are shown in Table 2.4. The parameters of three test cases (t1, t2, and t3) are also shown in Table 2.4. For illustration, the electrical current to the TECs is fixed (at 4*A*) for all observations and test cases. Based on the inlet hydraulic diameter and the inlet velocity observations, the

Reynolds number of the observations ranges from 13,692 to 38,337. A 3-D segregated $k-\varepsilon$ turbulent flow model is used for the CFD/HT simulation.

Table 2.4 Observations for enclosure and plenum

| Index of observations and test cases | *Re* | $\overline{V}_{in}$ (m/s) | RPM | $\overline{T}_{in}$ (K) | Q(W) |
|---|---|---|---|---|---|
| 1 | 13692 | 0.75 | 2500 | 306.5 | 6 |
| 2 | 16430 | 1.00 | 2800 | 305.0 | 8 |
| 3 | 19168 | 1.20 | 3200 | 303.5 | 10 |
| 4 | 21907 | 1.50 | 3500 | 302.0 | 12 |
| 5 | 24645 | 1.75 | 3800 | 300.5 | 14 |
| 6 | 27383 | 2.00 | 4200 | 209.0 | 16 |
| 7 | 30122 | 2.25 | 4500 | 207.5 | 18 |
| 8 | 32860 | 2.50 | 4800 | 206.0 | 20 |
| 9 | 35599 | 2.75 | 5200 | 204.5 | 22 |
| 10 | 38337 | 3.00 | 5500 | 203.0 | 24 |
| t1 | 26014 | 1.90 | 4000 | 299.6 | 15 |
| t2 | 33956 | 2.60 | 5000 | 295.4 | 21 |
| t3 | 20994 | 1.40 | 4700 | 297.0 | 19 |

The normalized velocity eigenvalue spectrum is shown in Figure 2.8. The rapid decay of $\lambda$ indicates that the first four or five POD modes capture the dominant 'kinetic energy' of the system and are able to construct the flow field with high accuracy. This is verified by the approximation error shown in Figure 2.9, which shows the errors for all three test cases become invariant beyond four or five POD modes. It is noted that the error for test case 3 is increased noticeably from mode 4 to mode 5. This is because the weighted coefficients of POD modes are obtained simultaneously by solving Equation (2.9), which does not necessary mean the approximation error will decrease monotonically with the addition of modes. For the flow field inside the enclosure, the approximation errors for all three test cases are less than 4.5%. An approximation error less than 3.5% is achieved with four or five POD modes for the plenum. The approximation errors of the temperature field are shown in Figure 2.9(b). Again, the data show that the approximate solution converges with 4 or 5 temperature modes, with an error of less than 8% for enclosure domain, compared to 6% for plenum domain. A possible reason that the plenum has lower approximation error for temperature field is that more accurate approximation of velocity field is achieved for the plenum domain.

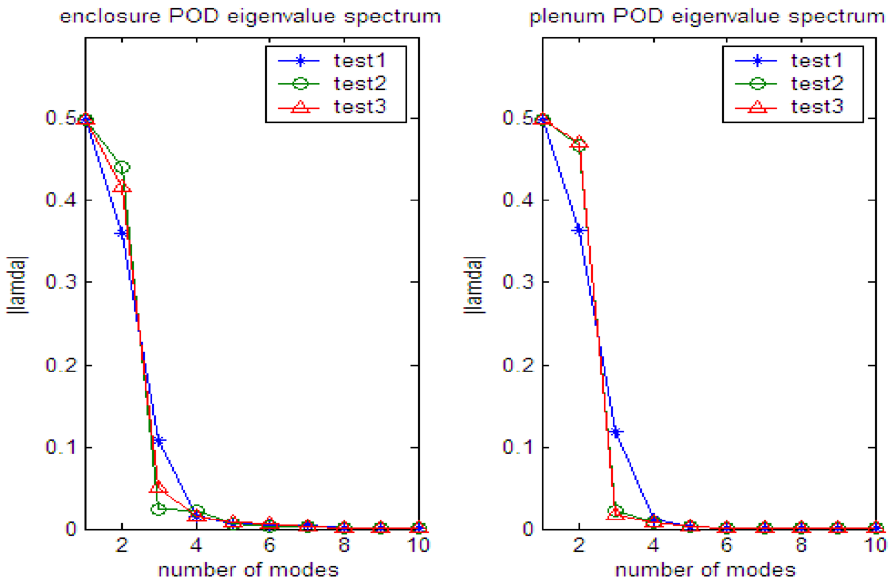



Figure 2.8 Velocity modal spectra for the POD procedure.

The cumulative ‘energy’ corresponding to the POD modes for velocity and temperature fields for test case 1 is shown in Figures 2.10 and 2.11, separately. For the flow field, modes 1 and 2 capture the dominant flow pattern, and mode 5 captures the circulation characteristics of the flow, compared to the full-field solution shown in Figure 2.12. It should be noted that this circulation is not noticeable in the full approximate solution due to its much smaller weighted coefficient. Similarly, for the temperature field, the first two modes capture the most information about the solution space, and mode 5 captures the temperature information around the package and TEC, compared to the full-field solution shown in Figure 2.13. The comparison between the reconstructed flow and temperature fields and results of detailed CFD/HT simulations is shown in

Figures 2.12 and 2.13, respectively. A close agreement is achieved for both flow and temperature fields, which makes it feasible to construct modular reduced order models to be used for cabinet level analysis.

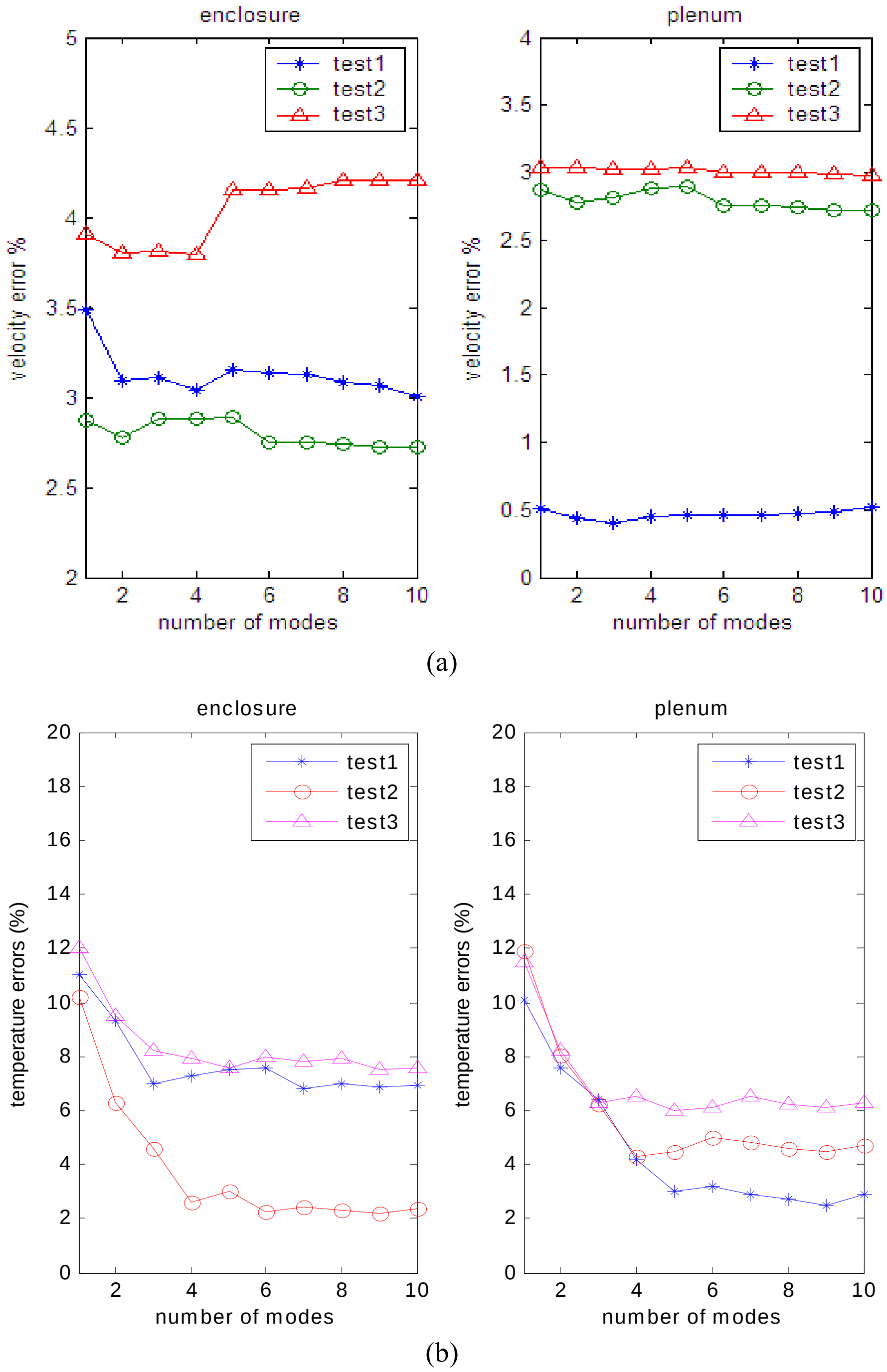
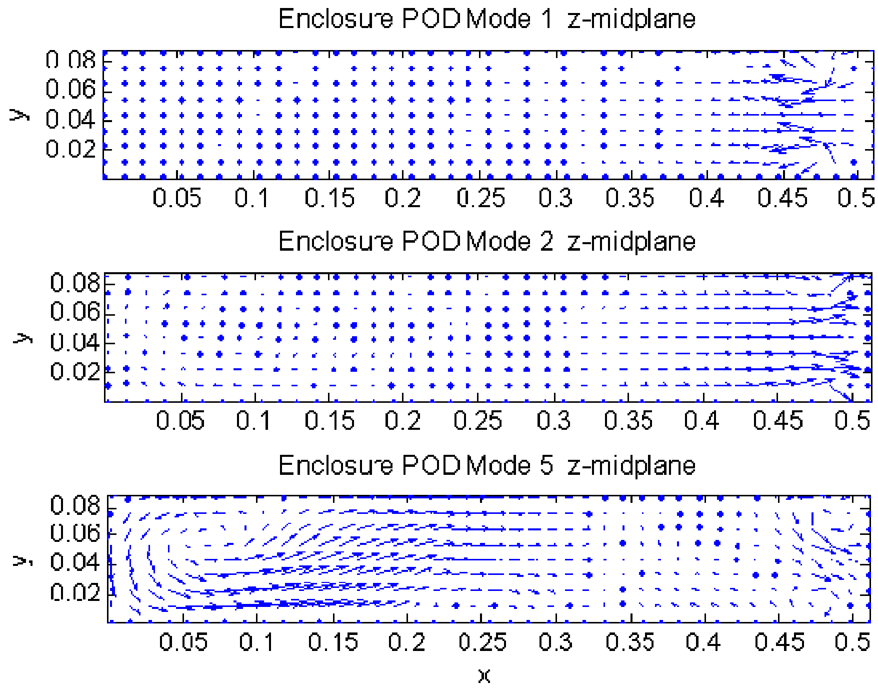
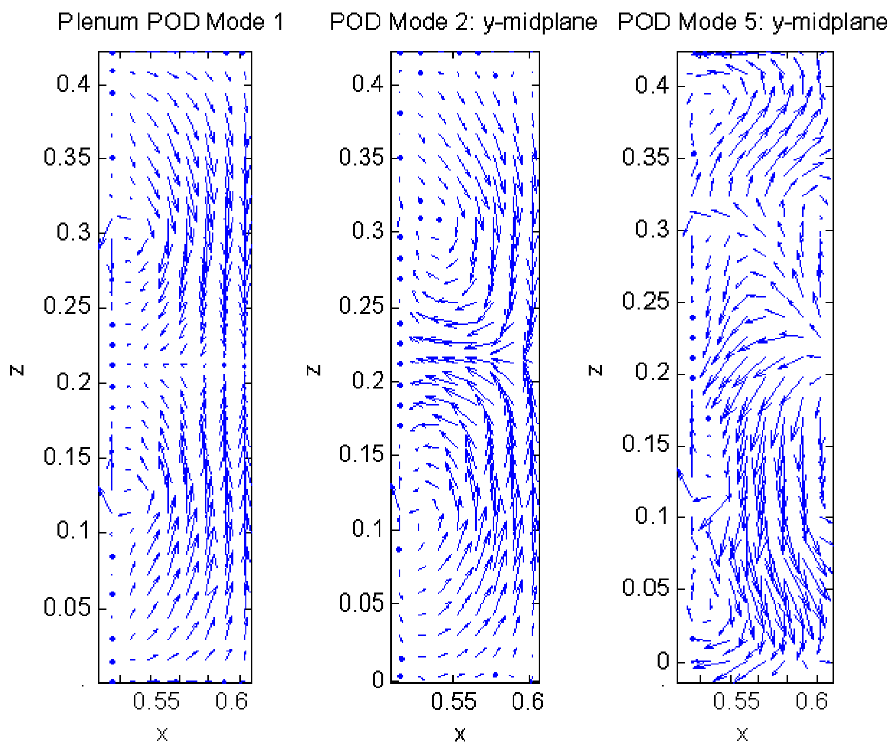



Figure 2.9 POD errors with number of modes (a) velocity field (b) temperature field. Conditions for the three test cases are listed in Table 2.4.




(a)




(b)

Figure 2.10 POD velocity modes: (a) enclosure, and (b) plenum, for test case 1, whose condition is shown in Table 2.4.

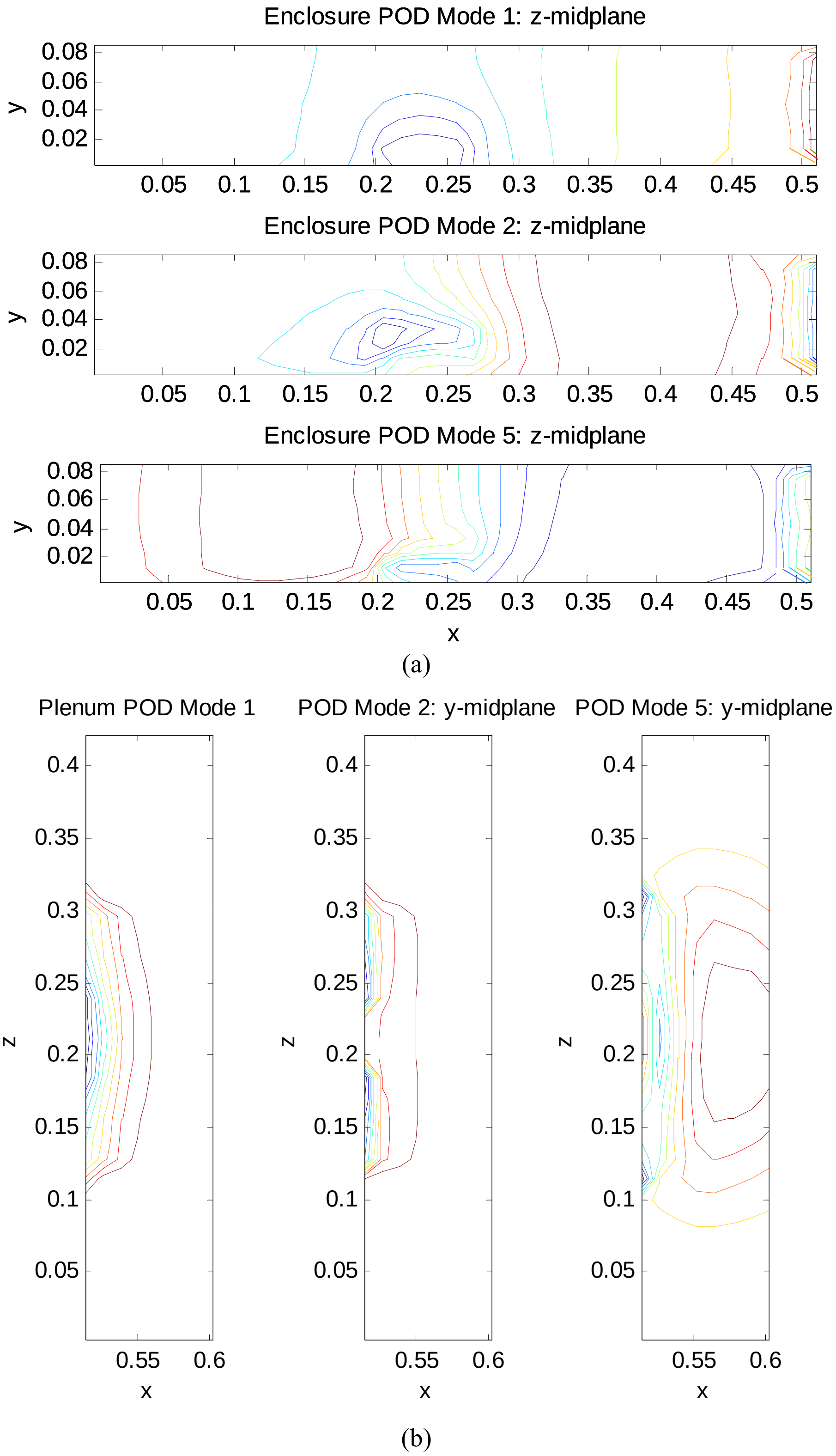



Figure 2.11 POD temperature modes: (a) enclosure, and (b) plenum, for test case 1, whose condition is shown in Table 2.4.

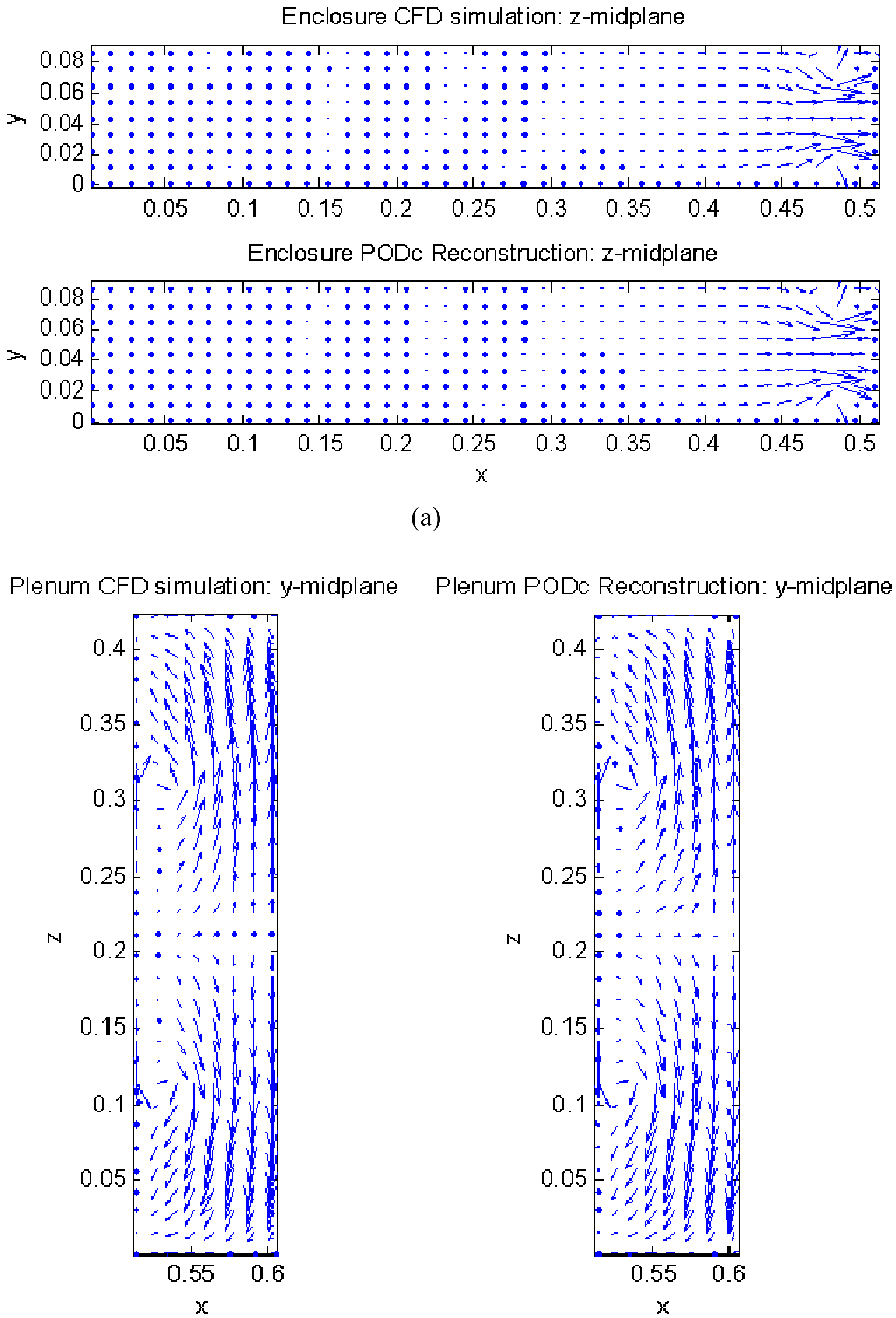
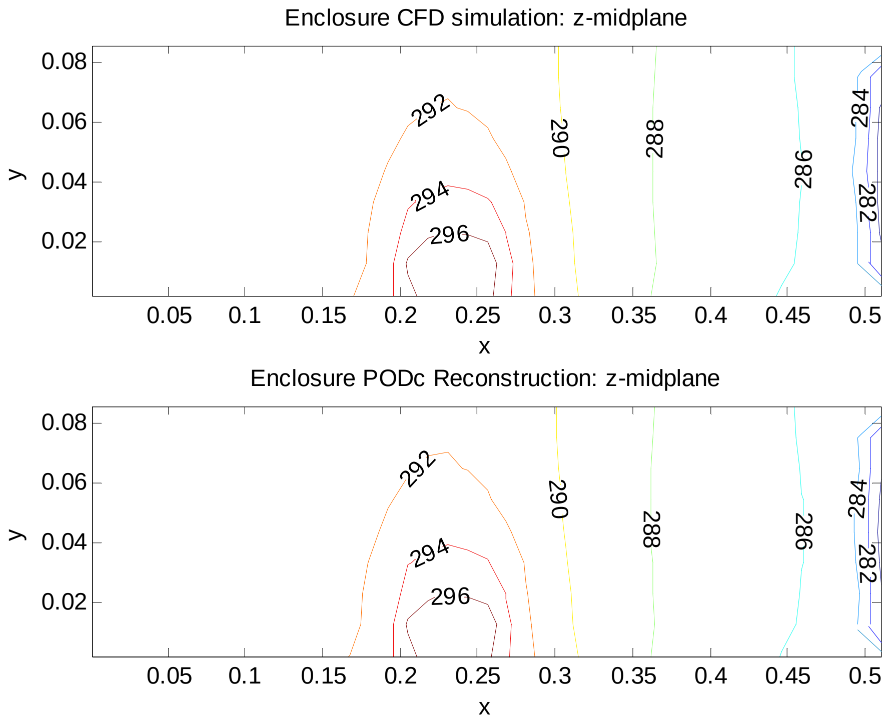
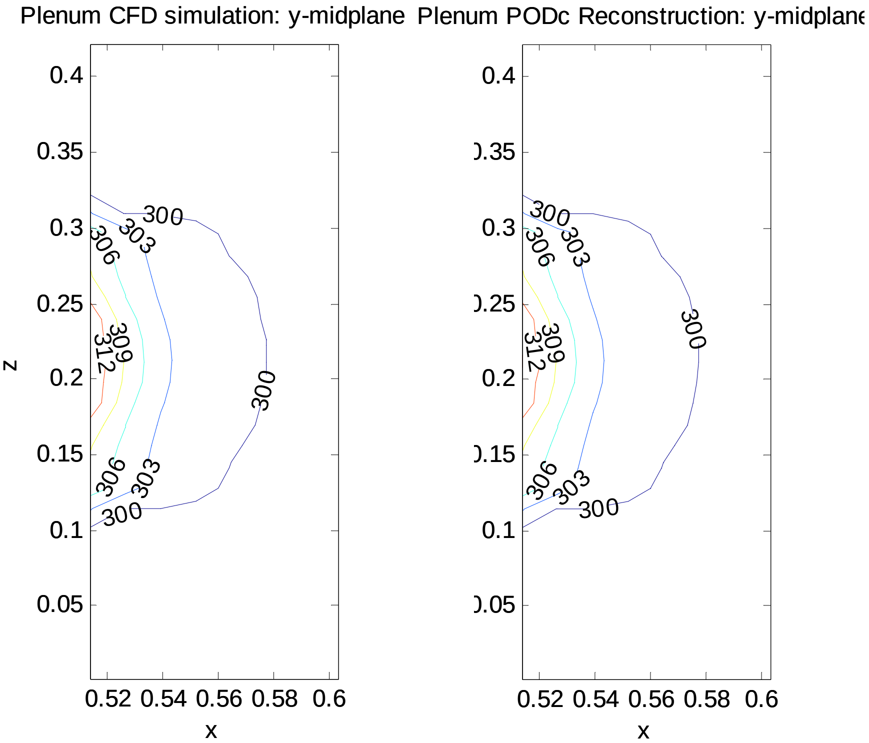



Figure 2.12 Reconstructed and CFD/HT velocity field: (a) enclosure, and (b) plenum, for test case 1, whose condition is shown in Table 2.4.




(a)




(b)

Figure 2.13 Reconstructed and CFD/HT temperature contour: (a) enclosure, and (b) plenum, for test case 1, whose condition is shown in Table 2.4.

## 2.7 Multi-scale Thermal Modeling for Electronics Cabinet

Starting with the compact model for a single enclosure subsystem, the compact model for the entire cabinet is generated by stacking multiple such enclosures. The mass and heat flow rate at the outlet of plenum domain are given by

$$F_{m,out}(\mathbf{u}) = \int_{\Gamma_{m,out}} \rho \mathbf{u} \cdot \mathbf{n} dA, \tag{2.25}$$

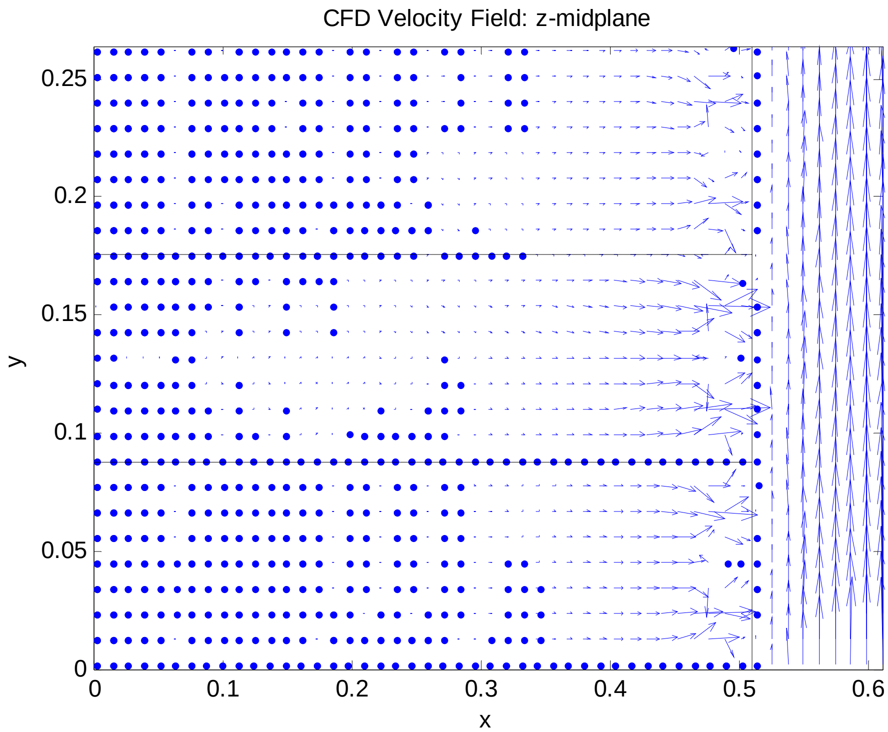
$$F_{h,out}(T) = \int_{\Gamma_{h,out}} \rho c_p \mathbf{u} T_{out} \mathbf{n} dA \tag{2.26}$$

respectively. These two outputs are taken as the input information for the next enclosure subsystem. This process proceeds until the last enclosure is stacked. A cabinet with three enclosures is studied with specifications shown in Table 2.5.

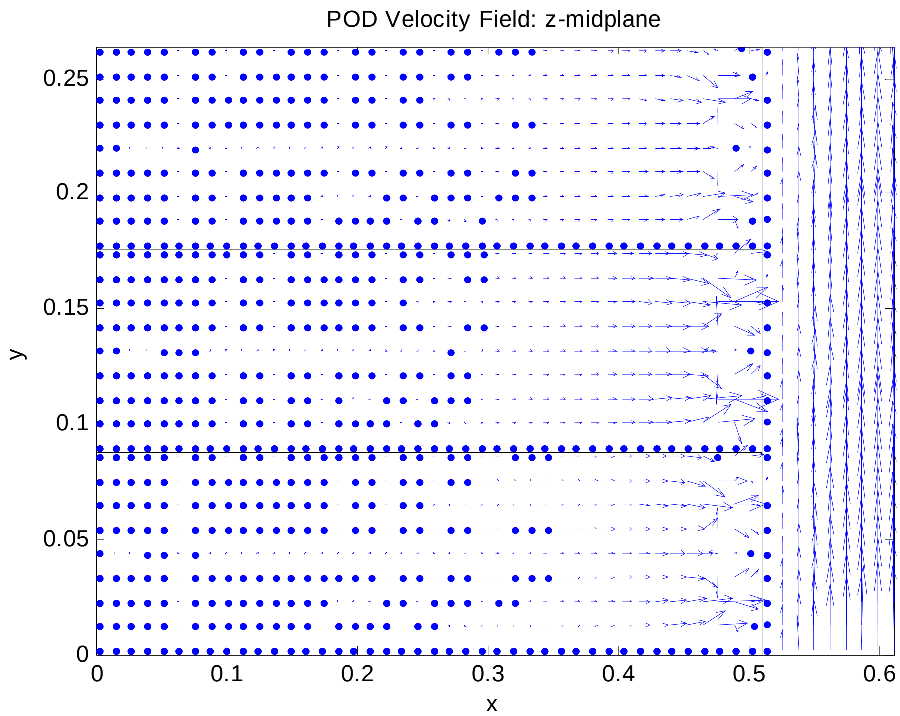
Table 2.5 Observations for cabinet

| Enclosure# | 1 | 2 | 3 | Cabinet Inlet | |
|---|---|---|---|---|---|
| RPM | 3900 | 4900 | 3000 | $V_{in}$ (m/s) | 1.9 |
| Q (W) | 15 | 21 | 9 | $T_{in}$ (K) | 298 |

Figures 2.14 and 2.15 show the POD reconstructed velocity and temperature contours at the vertical mid-plane of the cabinet, compared to full-field CFD/HT simulations. A noticeable agreement is achieved for the velocity fields inside all three enclosures, with a maximum approximation error of 4.5%. Since the velocity fields within and outside the enclosure are uncoupled, the accuracy of the compact model for the single enclosure is preserved during stacking. A somewhat larger approximation error, about 6%, is achieved for the flow fields in the plenum. This is because the flow boundary layer information is not captured in the POD based reduced order modeling. The same holds for the temperature field in the plenum. The approximation errors in the flow field resulted in even larger errors, 10% in current test cases, for the major domain of the temperature field, which is seen from Figure 2.15. Better agreement between the

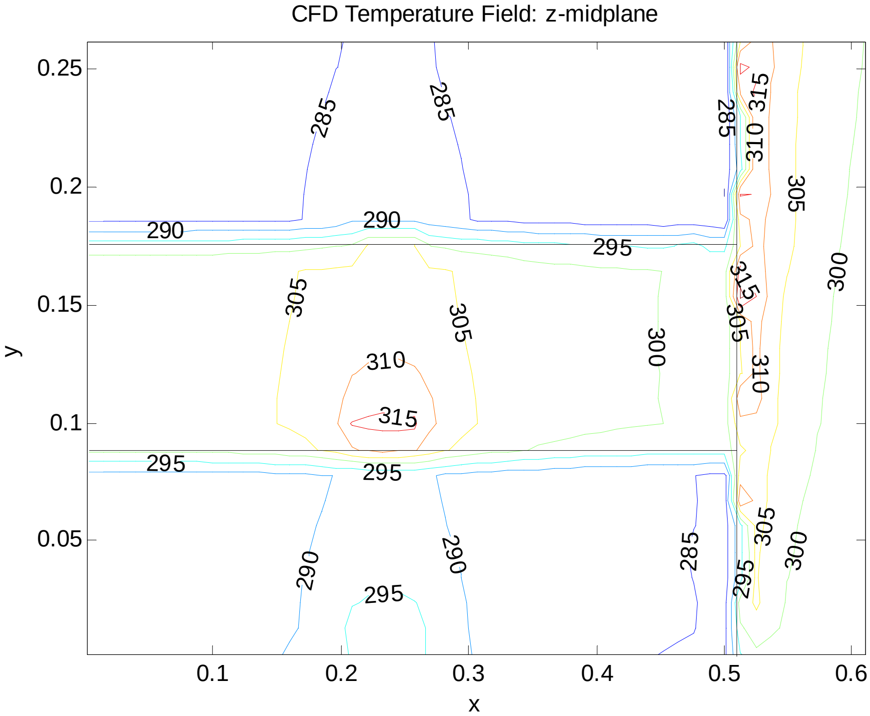



(a)

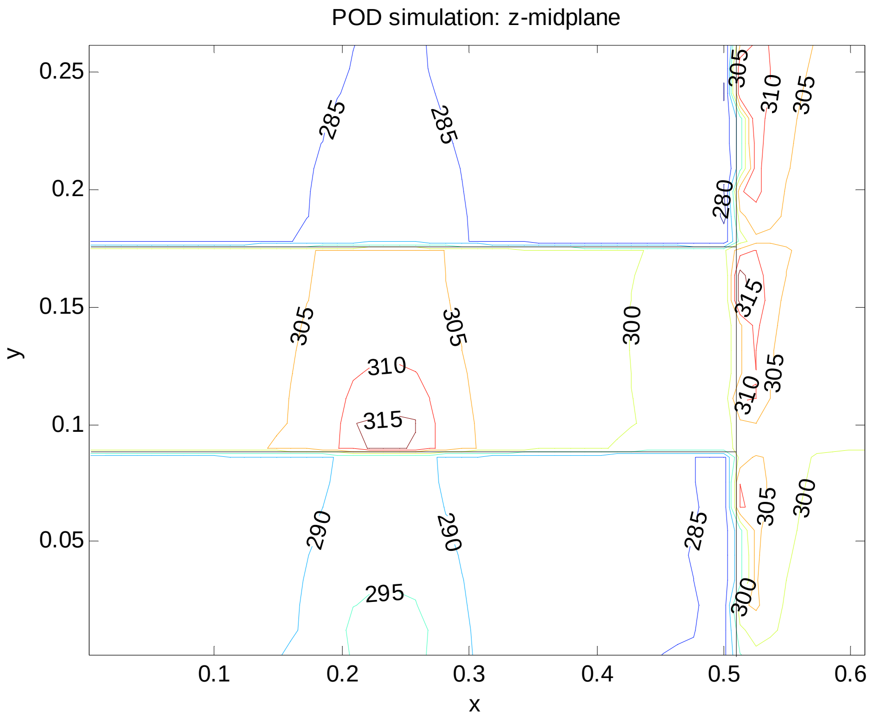



(b)

Figure 2.14 Simulation comparison of velocity field for the cabinet: (a) CFD/HT velocity contour, (b) POD velocity contour, at the vertical mid-plane.




(a)




(b)

Figure 2.15 Simulation comparison of temperature field for cabinet: (a) CFD/HT temperature contour, (b) POD temperature contour, at the vertical mid-plane.

POD based solutions and CFD/HT solutions was achieved for the temperature fields inside the enclosures, due to the more accurate POD approximation for the velocity field inside the enclosures. This is desirable since the chip junction temperature is more important for electronic cabinets.

The full CFD model for a single enclosure subsystem contains 135,671 grid cells with 7 degrees of freedom (DOF) per grid cell ( $P, u, v, w, k, \varepsilon$ and $T$ ). Therefore there are 949,697 degrees of freedom (DOF) for the fluid dynamics and heat transfer for a single enclosure subsystem, compared to 10 DOF (10 modes) with the POD method. The DOF of the system was thus reduced by almost 5 orders of magnitude. The results from POD method could be obtained in 3 minutes compared to 3 hours in the case of full CFD model of a single enclosure subsystem with a Pentium® 4 CPU 2.8 GHz computer. About 2 hours and 15 minutes are still needed for the full CFD model to get converged in the case of coarse mesh (99,850 grid cells). Therefore, the POD method shows superior performance over the full CFD simulation in the parametric studies during system prototype design.

As mentioned above, the current methodology based on POD cannot capture the boundary layers, especially the thermal boundary layer (see Figures 2.15(a) and (b)) in the plenum part due to the fact that the inputs to the numerical model with POD are typically in the integral format of variables such as mass or heat flow rate, instead of velocity or temperature profile. This will limit the application of POD on the modeling of multiple interconnected domains. However, this problem can be alleviated by taking the boundary profile into account when generating the system observations, which will be described in Chapter 4.

# CHAPTER 3

# ZOOM-IN REDUCED ORDER THERMAL MODELING OF MICROSYSTEM ENCLOSURE

A framework of multi-scale thermal modeling of electronic system is introduced in Chapter 2. A thermal modeling capability from 'chip-to-system' has been achieved with that framework. Essentially, that framework is based on the modular design by developing compact model for component and constructing reduced order model for subsystem. Reasonable level of approximation accuracy can be achieved for various levels. However, accurate prediction of the temperature distribution inside the component may be necessary for the reliability analysis of the device. A compact model for the component may not seriously affect the system level simulation, but it may affect the temperature distribution within each material layer. In this Chapter, a two-step "zoom-in" reduced order modeling is presented. With this approach, computational cost is significantly reduced, compared to conventional single-step computational thermal modeling, while the temperature distribution inside each material layer can be obtained.

## 3.1 Zoom-in Reduced Order Modeling

The general approach of zoom-in based reduced order modeling for the thermal analysis of electronic system is shown in Figure 3.1. Multi-layer compact models are developed for the components inside the system, and are used to replace the detailed component during the system level simulation. A POD based reduced order model for the system with compact components is developed. Necessary thermal information from the global model was extracted and used as boundary conditions for component level simulation. Detailed solution is realized at both system level simulation and component level simulation through this "zoom-in" approach.

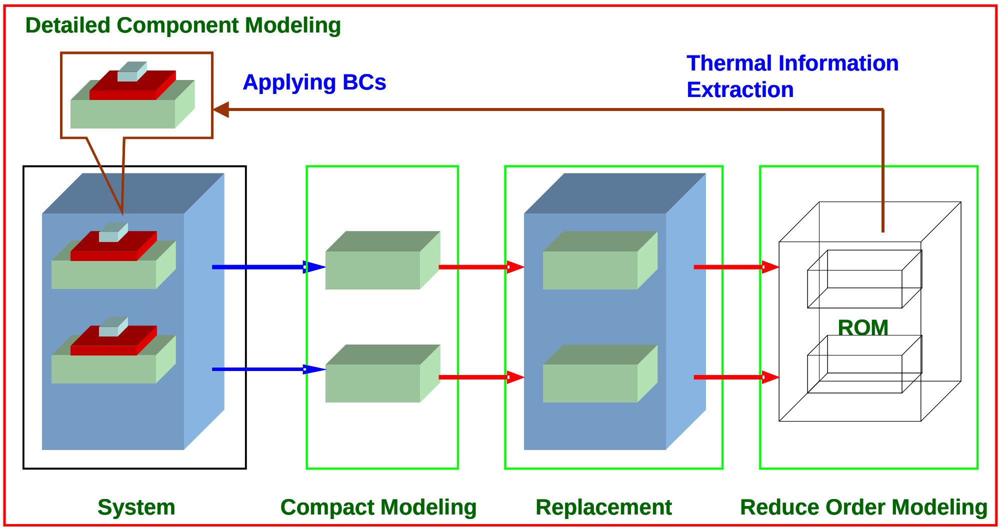



Figure 3.1 Zoom-in reduced order modeling

## 3.2 Case Study

### 3.2.1 System Description

For the demonstration, a microsystem enclosure with component was investigated, as shown in Figure 3.2. It is a standard EIA 1U computation server enclosure with one plastic quad flat package (PQFP) chip amounted onto the printing wiring board (PWB). Air enters the enclosure through the left side of the enclosure and runs across the PWB and chip package, then exits on the right side. A copper heat spreader and a longitudinal aluminum heat sink are attached to the top of the chip. The chip package is located in the centerline of z direction, which is z=0.212m.

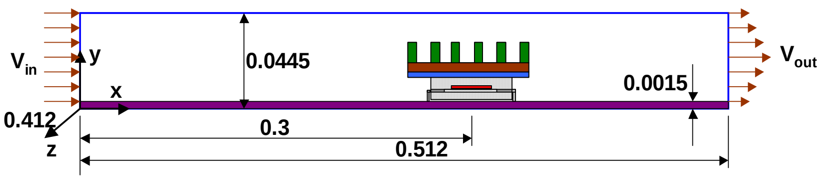



Figure 3.2 Sketch of the forced air-cooled enclosure system.

### 3.2.2 Zoom-in Reduced Order Modeling Procedure

This multiscale thermal modeling methodology here involve a sequential two-step "zoom-in" approach to resolve both the large scales associated with the microsystem enclosure, and the smaller length scales associated with fine spatial structures of the package component inside the enclosure. Specifically, a compact model of the package capable of accurate junction temperature prediction is developed at first, and is used in the system level CFD simulation. The thermal information, such as temperatures, heat flux or heat transfer coefficients, from the global model based on POD reduced order modeling is extracted and used as boundary conditions for component level simulation. The procedure for this methodology is shown in Figure 3.3.

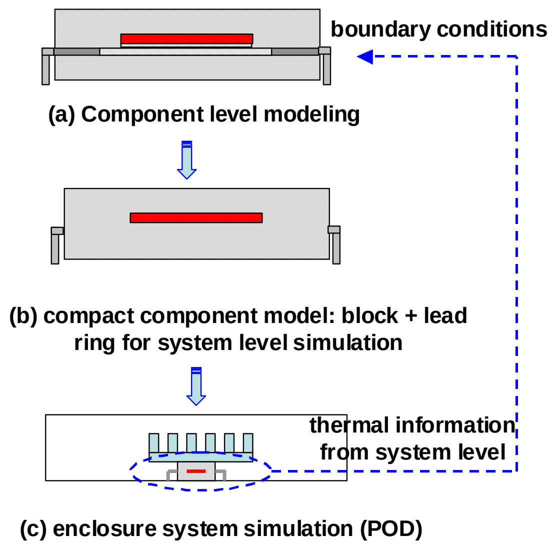



Figure 3.3 Procedure of zoom-in reduced order thermal modeling

### 3.2.3 Compact Thermal Modeling for PQFP Chip

Figure 3.4 depicts the geometry and layout of the PQFP used for detailed simulations. This detailed model has been widely used to simulate the prototype PQFP [24, 27, 74-76]. Some compact models have been developed to predict its thermal behavior [24, 27]. Those models, however, are only tested in the cases without attached heat spreader or heatsink. Figure 3.5(a) shows one of those models. A uniform effective thermal conductivity based on the volume average was used for the compact model in their simulations. This will under-predict the junction temperature of the chip with heat spreader or heatsink on the top. This is because the dominant heat path will be from the die to the top surface, and the much larger effective thermal conductivity than the encapsulant will result in much lower chip junction temperature. A new compact model is therefore necessary to handle this case.

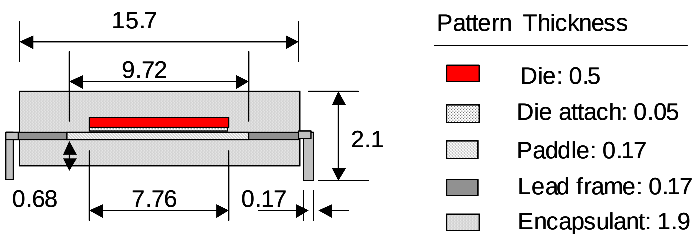
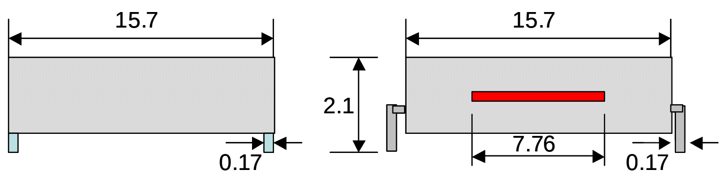



Figure 3.4 Package geometry and dimensions used in the detailed model. All dimensions are in millimeters.

A block with die and lead-ring compact model, which is shown in Figure 3.5(b), was used to simulate the detailed model shown above. Although the model looks more complicated than the block-on-lead model, it is still simplified enough, compared to the detailed model. The benefits of utilizing this type of compact model in the system level simulation are the velocity profile in the enclosure flow domain will be preserved, and temperature profile can also be closely maintained.




(a) (b)

Figure 3.5 Compact models, (a) block-on-lead model [24] and (b) block with die and lead-ring model.

The next key step is to determine the effective thermal conductivity of the compact model. From the previous discussion, it is better to use a non-uniform thermal conductivity to achieve a boundary condition independent compact model. The volume, excluding the die, averaged thermal conductivity is used for the lateral thermal conductivity of the block:

$$\kappa_{//} = \frac{\kappa_{lead\_frame}V_{lead\_frame} + \kappa_{die\_attach}V_{die\_attach} + \kappa_{paddle}V_{paddle} + \kappa_{encapsulant}V_{encapsulant}}{V_{lead\_frame} + V_{die\_attach} + V_{paddle} + V_{encapsulant}} \quad (3.1)$$

where $\kappa$ is thermal conductivity and V is volume. The original encapsulant thermal conductivity is taken as the perpendicular thermal conductivity of the block. Table 3.1 shows the thermal conductivities used for the detailed model and compact models.

Table 3.1 Thermal conductivities used for models

| Materials | $\kappa_{//}$ *(W/mK)* | $\kappa_{\perp}$ *(W/mK)* |
|---|---|---|
| Compact block (b) | 13.5 | 1.0 |
| Compact block (a) | 26.6 | |
| Air | 0.0263 | |
| PWB | 1.0 | |
| Encapsulant | 1.0 | |
| Die | 148 | |
| Die attach | 1.0 | |
| Lead frame mixtures | 138.5 | |
| Lead ring | 138.5 | |

To test the accuracy of the block with die and lead-ring model, rather than using the exhaustive set of boundary conditions proposed in [77] (38 sets in all), only 8 different sets (combination of adiabatic, isothermal, isoflux and constant convection heat transfer coefficients on the package surfaces). The boundary conditions used for each set are shown in Table 3.2.

Table 3.2 Boundary conditions used for model test

| BC Set No. → <br> Package Surface ↓ | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Top | T | A | T | A | T | q | T | h |
| Bottom | A | T | T | T | T | T | A | T |
| Sides and Leads | A | A | A | T | T | A | q | A |

where T=isothermal (300K), A=adiabatic, q=isoflux (-200 W/m$^2$), h=convection heat transfer coefficients (40 W/mK).

Table 3.3 Comparison of compact models and full model

| T and Q → <br> Method ↓ | $T_j$ | $Q_{top}$ | $Q_{bot}$ | $Q_{side+leads}$ |
|---|---|---|---|---|
| Compact (a) | 95 | 15 | 21 | 51 |
| Compact (b) | 8.5 | 2.1 | 3.0 | 3.5 |

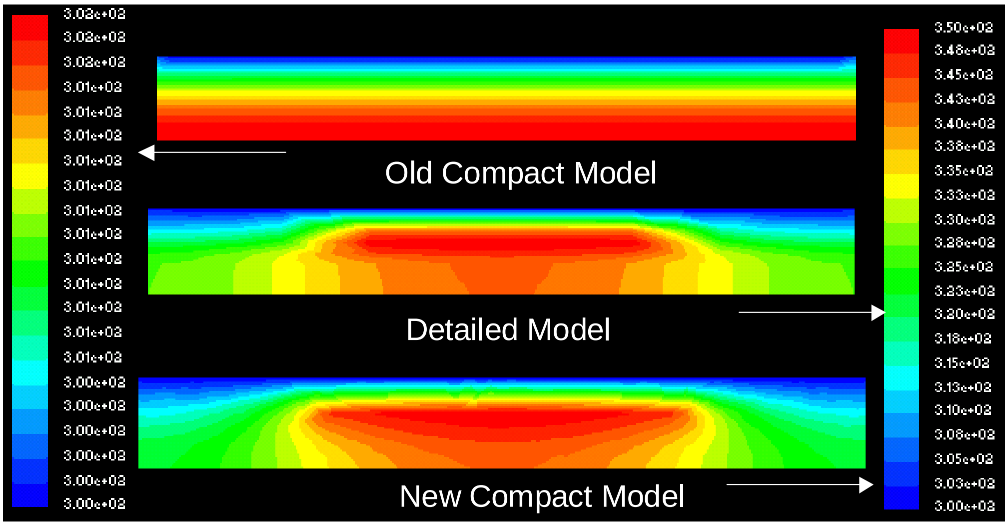



Figure 3.6 Temperature profiles for compact model (b) and detailed model with BC#1 (Q=24W)

The maximum relative errors in junction temperature and thermal budgets of the compact models compared to the detailed model are shown in Table 3.3. It can be seen that very accurate predictions have been achieved for the chip package with current compact model, especially for the thermal budget. The maximum errors (8.5%) occurs where the sides and leads are in isothermal or isoflux conditions. The minimum error (less than 1%) occurs where the top surface is in non-adiabatic conditions. For the forced air-cooling with heat sink, the heat flow path along top surface dominates the thermal budgets, about 90% in our case. Therefore, this compact model is very accurate in the system simulations of this case. The temperature profiles of both detailed model and compact model are shown in

Figure 3.6, which implies that the major profiles match very well. The previous block-on-lead model has much larger errors and the temperature profile is totally different from full model. Since the thermal performance of the new compact model is very close to the detailed model, it can be used to replace the detailed model in the system level (enclosure level in this case) simulation to save computational time.

### 3.2.4 System Level Simulation

Ten observations for the enclosure system are generated and shown in Table 3.4. The Reynolds number of the observations ranges from 2,457 to 13,513. A 3-D segregated k-ε turbulent flow model is used for the CFD system level simulation with Fluent 6.1.

Table 3.4 Observations for the enclosure system

| Cases | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | t1 | t2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vin (m/s) | 0.5 | 0.75 | 1.0 | 1.25 | 1.5 | 1.75 | 2.0 | 2.25 | 2.5 | 2.75 | 0.9 | 1.9 |
| Q (W) | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 13 | 21 |

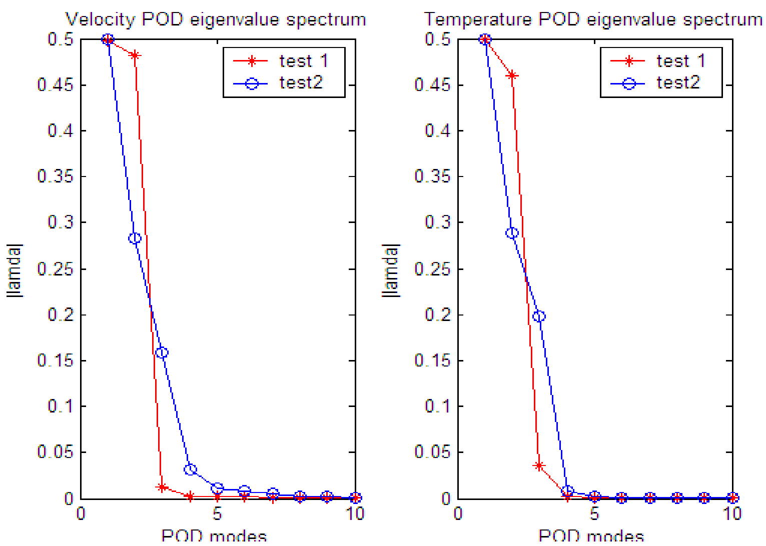



Figure 3.7 POD eigenvalue spectrum for test cases

The normalized eigenvalue spectrums for both velocity and temperature field are shown in Figure 3.7. Since each POD mode corresponds to an eigenvalue of the system and carries the system energy, the rapid decay of $\lambda$ indicates that the first four or five POD modes capture the dominant "kinetic energy" of the system and are able to construct the flow and temperature field with high accuracy. This can be seen from the relative errors of the approximated velocity and temperature fields, which are shown in Figure 3.8. The errors of both test cases are converged with p=4 or 5 modes, and the maximum error for velocity field is less than 2.7%, and 7.3% for temperature field.

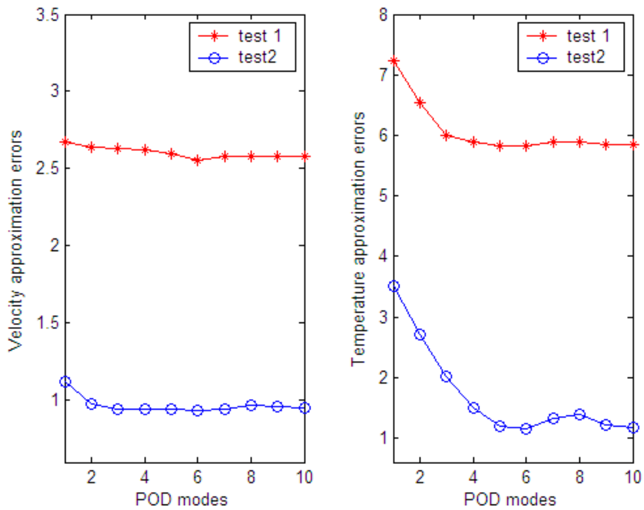



Figure 3.8 POD approximation errors vs. number of POD modes

From Figure 3.8, we can see the velocity approximation errors for both test cases are smaller than temperature approximation. This is partly because the temperature field is dependent on the velocity, and the velocity errors will propagate to the temperature field. Another reason is that the compact thermal model, instead of the detailed model, is used for the chip package in the system level simulation. As we mentioned earlier, this compact model does not affect the velocity field, but do affect the temperature field. Although the approximation errors in test case 1 is much larger than test case 2, this dose not necessarily mean that the case closer to the center observation will lead to smaller errors. POD can even reconstruct the test field outside the observation range with acceptable accuracy [29]. The POD modes corresponding to different "cumulative" energy of the system are shown in Figure 3.9 for both velocity and temperature fields of test case 2.

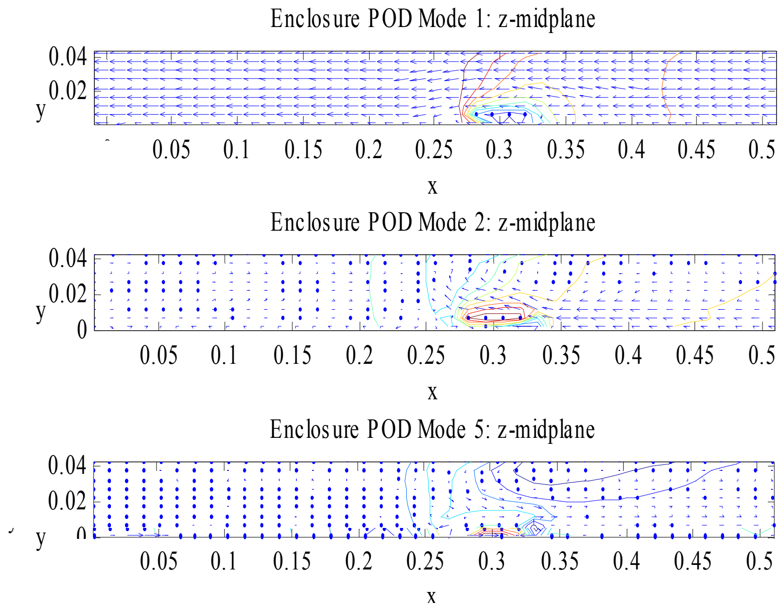



Figure 3.9 POD modes for velocity and temperature fields

It can be seen that the dominant flow pattern was captured by velocity POD mode 1, and mode 2 captures the circulation characteristics of the flow, compared to the true solution shown in Figure 3.10. For the temperature field, the first mode capture the most information of the solution space, and mode 2 make the contributions to the temperature around the chip package. The fifth mode of both velocity and temperature field makes no physical contributions.

The comparison between the POD reconstructed fields and the detailed simulations are shown in Figure 3.10. A very good match for the velocity fields is achieved and the reconstructed temperature field is also very close to the true field from detailed CFD simulations. This implies that the POD method based on the system level simulations with compact component model can predict both velocity and temperature fields very well.

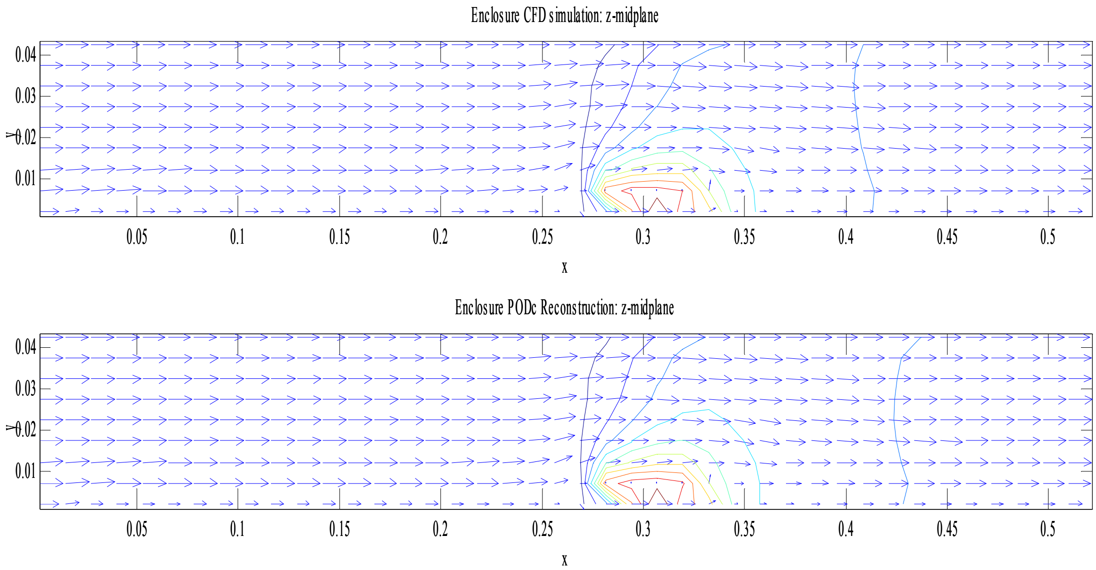


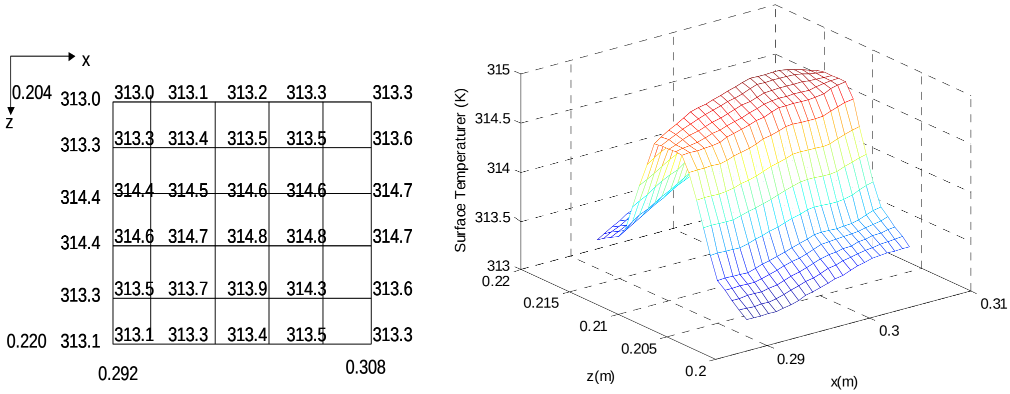

Figure 3.10 Comparison of reconstructed fields and CFD fields

### 3.2.5 Detailed Component Level Simulation

From the system level simulation results by POD method, the thermal information, such as temperatures, heat flux and local heat transfer coefficients, can be extracted and applied to the component as boundary conditions. This different thermal boundary information may affect the simulation results at the component level. Results for a leadless ceramic chip carrier (LCCC) chip imply that the combination of prescribed temperatures and heat flux may generate better results [75].

**(1) Data extraction and interpolation**

For the top surface of the PQFP component, only temperatures are extracted from the global model in current studies. When first extracted from system level solution, data were available on nine (5x5) internal discrete grid points, as shown in Figure 3.11(a). After cubic interpolation on a finer 23x23 mesh, the final representations for reference temperature are shown in Figure 3.11(b). These extraction and interpolation procedures are repeated for the bottom, sidewall and lead surfaces.



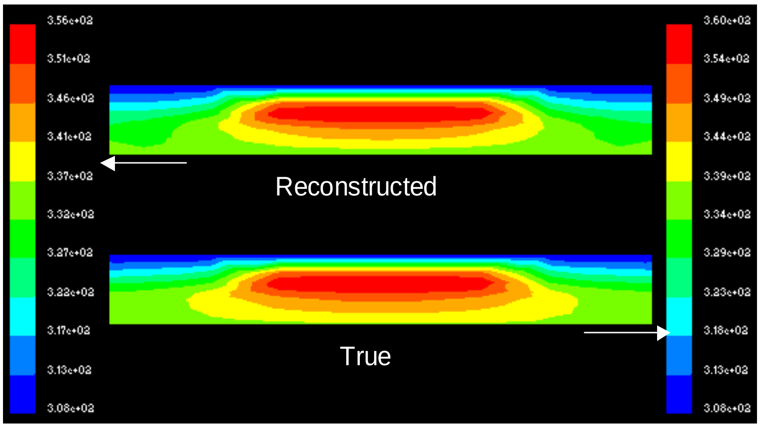

(a) (b)

Figure 3.11 Temperature for top surface of component (a) before interpolation, (b) after interpolation

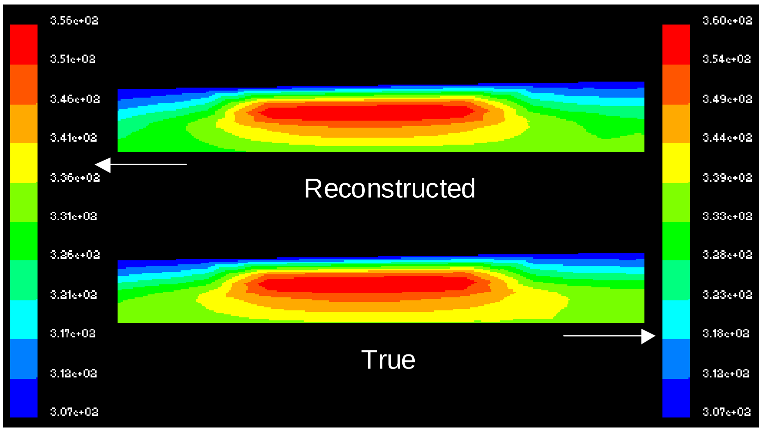
**(2) Detailed component level results**

With the thermal boundary information extracted from global model, there are two options for the component level simulations. One is to write the 3D conduction equations for the chip package, but it is time consuming. Another one is to use the User Defined Function (UDF) in Fluent. Specifically, all thermal boundary information is written into a single UDF function and then applied to the detailed model for the package in Fluent.

Figures 3.12 and 3.13 depict the comparison between the results from compact model and detailed model. For both test cases, a very good agreement between the compact model and detailed model is achieved, including both the temperature profiles and values. The maximum error for the junction temperature is less than 8.3% for test case 1 and 4.2% for test case 2. This validated our two-step "zoom-in" multiscale thermal modeling methodology.




(a)

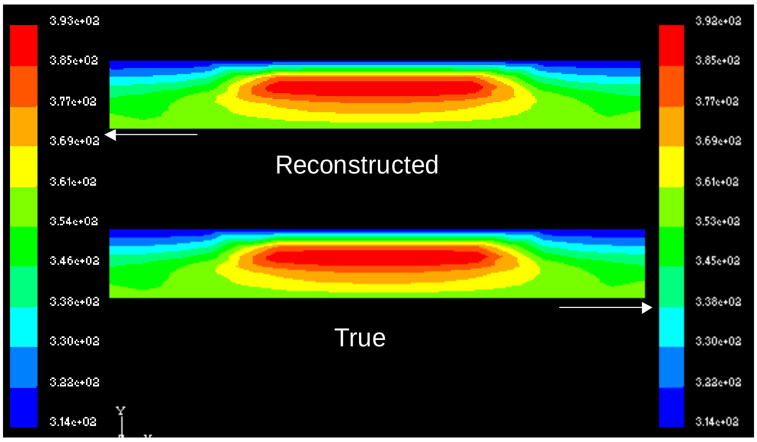



(b)

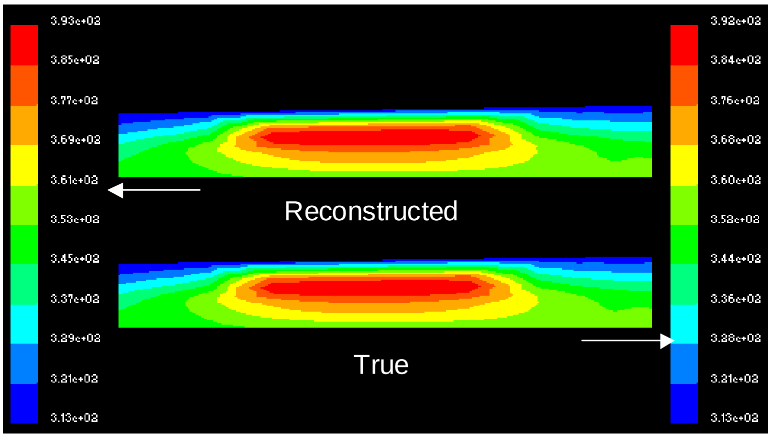
Figure 3.12 Comparison between compact model and detailed model for test case 1, (a) x-middle plane, (b) z-middle plane.

### 3.2.6 Computational Cost Analysis

The most potential advantage of this multiscale thermal modeling methodology is to save computational time, compared to detailed simulations. The number of nodes, running and post-processing time for both multiscale methodology and detailed CFD simulation method are shown in Table 3.5.




(a)




(b)

Figure 3.13 Comparison between compact model and detailed model for test case 2, (a) x-middle plane, (b) z-middle plane.

Table 3.5 Observations for the enclosure system

| Types | Multiscale Modeling | CFD Modeling |
|---|---|---|
| Number of nodes | 142305 | 251008 |
| Model construction time (hours) | 1 | 4 |
| Running time (hours/case) | 3.8 | 7 |
| POD running time (minutes) | 2 | NA |
| UDF simulation time (seconds) | 2 | NA |
| Total (hours) | 39 | 11 |
| Extra single simulation time (minutes) | 2 | 660 |

Although the multiscale thermal modeling takes longer time (most of it spent in generating the observations) than the detailed CFD modeling, it is superior over CFD simulation for any additional simulation.  For example, it only needs about 2 minutes for an additional solution, compared to 660 minutes with CFD simulation, reduced by two orders of magnitude. The advantages of the zoom-in multiscale thermal modeling here are more obvious when the system is in the prototype stage or parametric studies, in which many different cases may need to be simulated.  For example, if 20 cases need to be tested, then the time for the detailed CFD modeling will be around 148 hours, much larger than 39 hours with current method. Another appealing aspect of this methodology is that a complete multiscale thermal model may become possible for complex electronics system.

### 3.3 Extension of Current Methodology

Figure 3.14 shows the extension of our current methodology to both higher and lower scales thermal modeling of a data center. It is impossible to do a detailed CFD simulation for such a system with many length scales. Our current methodology provides a good starting point which can be easily extended to higher and lower scales.

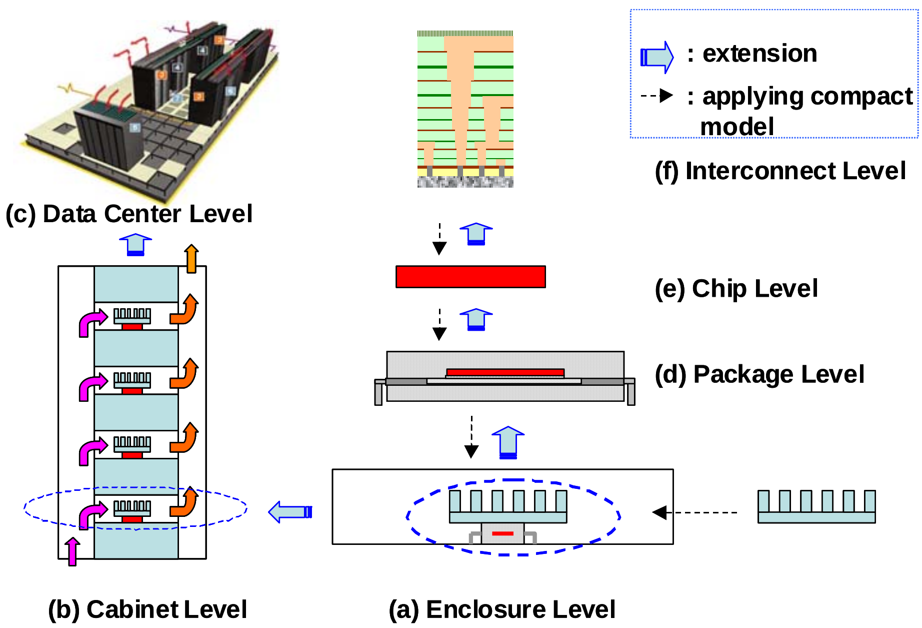



Figure 3.14 Extension of current methodology to different sales

# CHAPTER 4

# BOUNDARY MATCHING REDUCED ORDER MODELING AND EXPERIMENTAL VALIDATION

The reduced order modeling based on the module design concept described in Chapter 2 has been proved to be an efficient method for the multiscale thermal analysis of complex system consisting of a series of nested sub-domains. The ROM developed by POD is very convenient to conduct parametric study, due to its simple input-output characteristics. Also the ROM for each subsystem can be stored in the design library and reused in the current and future design and analysis. However, most current reduced order modeling based on the POD method focus limited boundary conditions, e.g. either uniform or predefined profile input/output [13, 54]. This seriously limited the application of ROM to the system level simulation, since the boundary conditions of thermal fluid sub-systems within a complex system are generally unknown profiles, instead of fixed variables. A POD based reduced order modeling approach with boundary matching technique is proposed in this chapter. Also an efficient handshaking scheme between ROMs based on the concept of flow network modeling (FNM) is developed. This approach was validated through experiments conducted on a air-cooled sever cabinet.

## 4.1 Reduced Order Modeling with Boundary Matching

### 4.1.1 Effect of Boundary Profile

To investigate the boundary effect on the reduced order modeling, consider a 2-D server model shown in Figure 4.1. Two simulations are conducted with two different boundary conditions. The first simulation assumes a uniform input at the inlet of the server, and the second one assumes a profile input but having the same average mass flow rate as the first case. All other boundary conditions remain the same for both cases. The flow and pressure fields of two cases are shown in Figure 4.2. The top two graphs show the results for the case with uniform input and the bottom two for the case with profile input. It can be seen both the velocity and pressure fields with profile input are quite different from those with uniform input, which indicates that the effect of the boundary profile is not negligible for CFD numerical simulation. Since CFD simulation or experiments is typically the first step for POD reduced order modeling of thermal fluids system, the effect of boundary profile on the reduced order modeling is obviously not negligible.

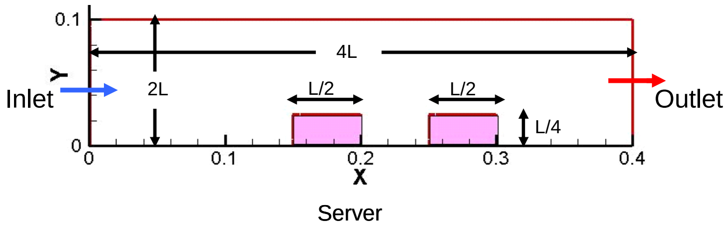



Figure 4.1 2-D server model

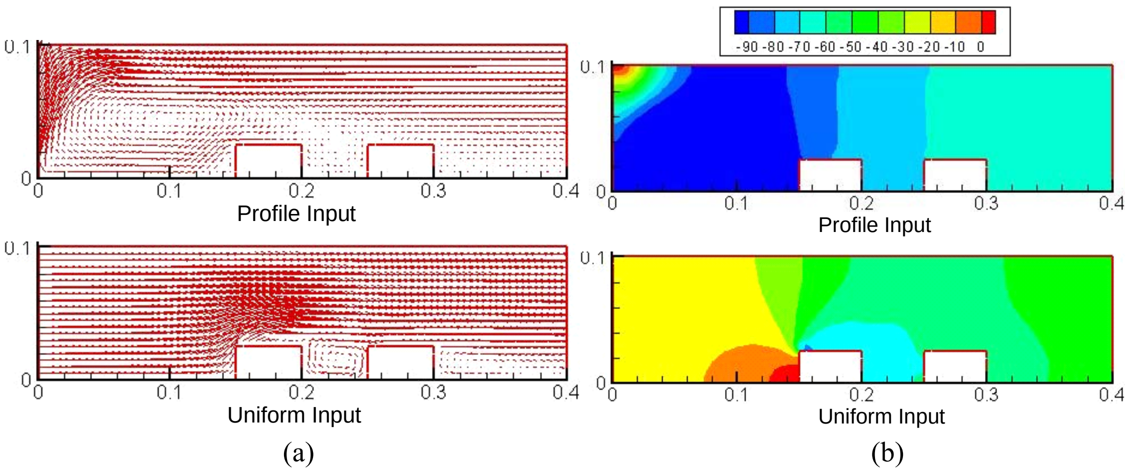



Figure 4.2 Comparison of profile input and uniform input: (a) pressure (Pa), (b) velocity

### 4.1.2 Boundary Profile Capturing Scheme

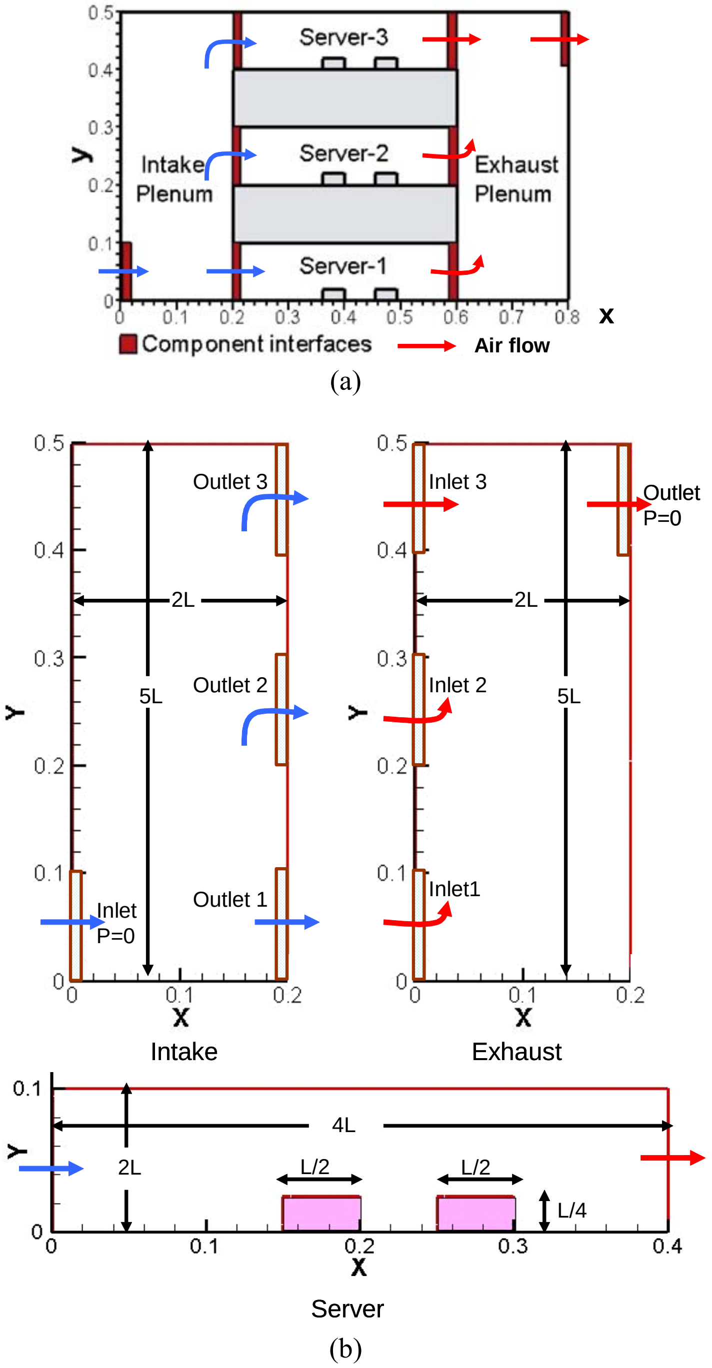
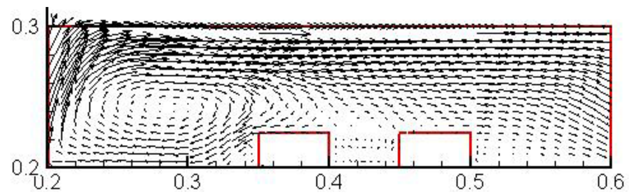


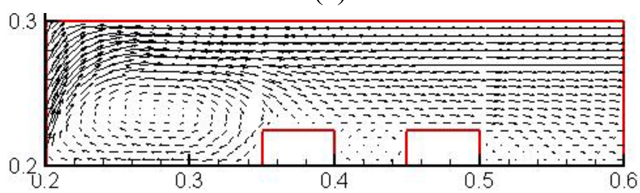

Figure 4.3 Two-dimensional rack model: (a) system model, (b) geometry of components

A typical way to capture the boundary profile is to utilize the output profiles of the sub-domain upstream as the inlet boundary profiles of sub-domain downstream.

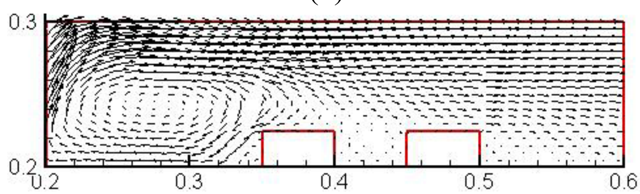
However, large errors may be incurred, since the sub-domains downstream may affect the flow pattern of the fluid at the exits of sub-domain upstream. To keep the flow pattern of the outputs of the sub-domain upstream close to the complete system, a flow straightening duct with the same cross-sectional geometry as the sub-domain downstream can be added to each outlet of the sub-domain upstream. For the demonstration, consider a highly simplified 2-D model of an air-cooled rack containing multiple servers and two plena at the intake and exhaust, as shown in Figure 4.3. To capture the profile input of the servers, the output put profile of the intake plenum can be taken as the input profile of the server models. Figure 4.4(a) shows the velocity input (real input) to the second server at system level simulation, and Figure 4.4(b) shows the velocity profile to the server obtained by extracting the output profile of the intake model when simulated separately. It can be seen that both results are kind close to each, which indicates the real velocity input to the second server can be approximated by the output profile of the intake model.




(a)

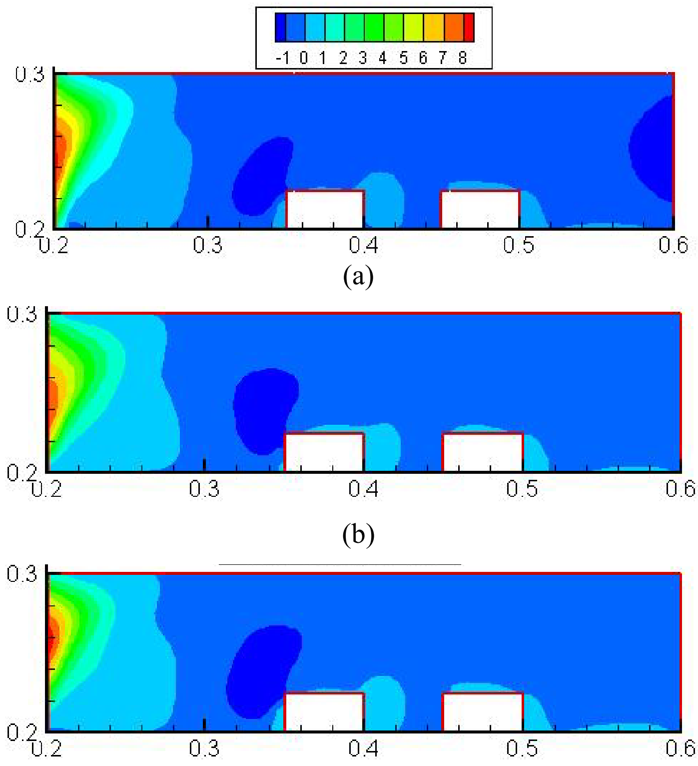



(b)




(c)

Figure 4.4 Velocity profile, (a) real input, (b) intake output w/o duct, (c) intake output w/ duct




(a)

(b)

(c)

Figure 4.5 y-velocity, (a) real input, (b) intake output w/o duct, (c) intake output w/ duct

A close examination of both velocity input profiles above indicates that the air recirculation in the server is not fully captured in Figure 4.4(b), especially, in the region around the first chip. This is expected because the server can conduct (bend) the air fluid exiting the intake model at system level simulation. To capture this effect, a flow straightening duct with the same cross-sectional geometry as the server is added to the outlet of the intake model, as shown in Figure 4.6. The velocity input profile to the server model after adding the flow straightening duct is shown in Figure 4.4(c). A more accurate velocity input profile to the server model has been achieved after adding the duct, compared to that without adding duct shown in Figure 4.4(b). This difference is more obvious from the y velocity contours shown in Figure 4.5 under these three cases. This indicates that the boundary profile can be captured with reasonable accuracy during the CFD simulation.

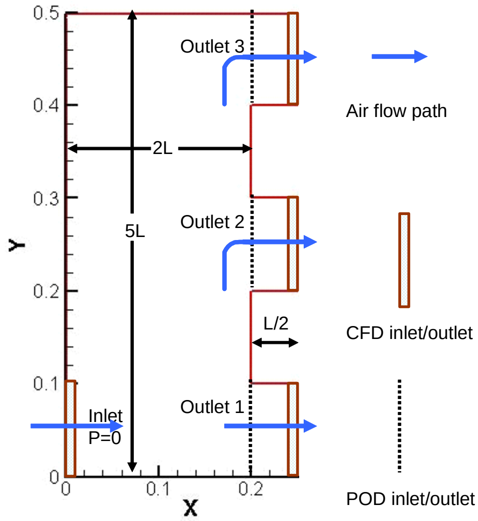



Figure 4.6 Flow straightening duct

As stated before, since CFD simulation is typically the first step of the POD reduced order modeling, it is possible to include the effect of the boundary profile in the POD reduced order modeling. However, the general inputs and outputs of the reduced order modeling are fixed variables for the sake of coding. For instance, the averaged mass flow rate (averaged velocity) is typically defined at the inlet of a system, and a total heat flow rate (averaged heat flux) is defined for a package. To include the effect of the boundary profile in the reduced order modeling, it is necessary to make an assumption that there is a unique map between the averaged variable values and the boundary profile. This assumption is reasonable for most thermal fluid systems. For instance, for the example shown in Figure 4.3, the general flow pattern of the input to the server will not change dramatically, unless the inlet of the intake is switched to the top. With this assumption, the boundary profile inputs are taking into account during CFD simulation for snapshot generation, and the averaged values of the boundary profile are used in the

POD reduced order modeling. The flux matching can also be utilized since the averaged values are used for the reduced order modeling.

### 4.1.3 Multiscale Thermal Modeling Methodology

Many electronics systems such as electronics cabinets are modular in nature, consisting of a series of nested sub-domains, as shown in Figure 4.1. The general approach here is to divide such system into multiple sub-domains or subsystems. A POD based reduced-order model (ROM) with input and output information is constructed for each subsystem separately and subsequently linked together to model the complete system, as shown in Figure 4.7 for the demonstrated example. It is noted that the boundary effect is included in this methodology by adding necessary duct to the outlet of the subsystems upstream.

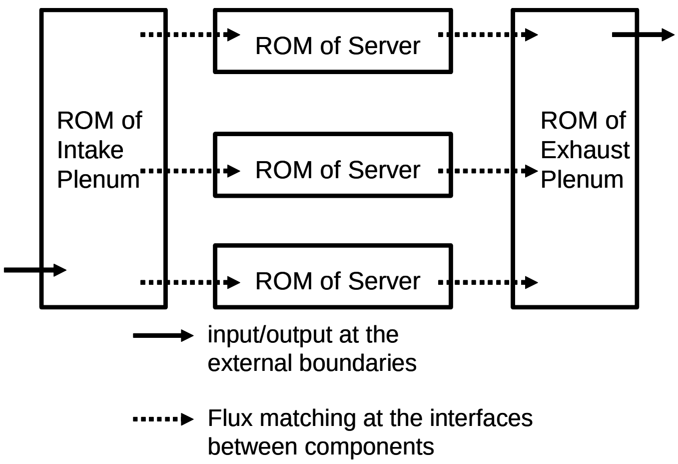



Figure 4.7 Reduced order modeling methodology

To assemble the full system with ROMs for the system components, concepts from FNM [12, 78, 79] are used to generate the matching conditions between the interfaces of those ROMs. Each system component is represented by a combination of links and nodes. Pressure and temperature are calculated at each node characterized by conservation law.

$$\sum_i G_{m,i} = 0 \text{ and } \sum_i G_{h,i} = 0 \tag{4.1}$$

for mass and energy, respectively, while the flow rates are associated with links characterized by the following momentum equation

$$P_1 - P_2 = \Delta P = f(G_m) = K_1 G_m{}^2 + K_2 G_m \tag{4.2}$$

The pressure loss coefficient $K_1$ and $K_2$ here for standard components (screens, ducts, bends, etc) can be found from handbooks or Moody chart [80]. For non-standard components, experimental data or CFD simulations can be used to get the flow characteristics. With POD method, CFD snapshots for each component can be used to obtain the flow characteristic of each component without introducing extra computational cost. A flow resistance network can be constructed with those links and nodes for the entire system. Linearization of Equation (19) is necessary to solve this network [78]

$$P_1 - P_2 = \Delta P = S_c + S_p G_m \tag{4.3}$$

where

$$S_c = (1 - (\frac{d\Delta P}{dG_m})^*)G_m^* \text{ and } S_p = (\frac{d\Delta P}{dG_m})^* \tag{4.4}$$

The '*' here represents the value at current iteration.

The standard SIMPLE algorithm [78] is used to solve for the nodal pressure, momentum link flow rates and the energy flow rates. The procedure is completely analogous to pressure-velocity coupling methods in incompressible CFD and is outlined here with more details available in [81]:

FNM – SIMPLE Algorithm

1. Assume a nodal pressure distribution and a link mass flow rate distribution.

2. Use the momentum link equations $\Delta P = f(G_m)$ to calculate the momentum link flow rates given the nodal pressures.
3. Construct a pressure correction equation by combining the corrected momentum and continuity equations. Solve the pressure correction matrix through direct method, and update the pressure and flow rates.
4. Repeat steps 2 to 4 till convergence
5. Solve the velocity and temperature fields with POD, given the link flow rates and heat loads; solve the pressure fields with response surface method, given the link flow rates

### 4.2 Pressure Field Approximation

Since many flows in electronic systems are pressure-driven, such as fans moving air through a series of channels, it is necessary to calculate the pressure field. However, one property of POD analysis is the elimination of pressure for incompressible flow. In theory, the flux matching technique can be extended to include the pressure term if the pressure boundary conditions are known. However, only boundary velocity or flow rate is available for many thermal-fluids systems. The response surface methodology can be used to deal with this case [29], where the pressure POD modes are projected back onto the pressure observations ensemble $\mathbf{P} = \{P_1, P_2, ..., P_n\}$ to obtain the set of observation weight coefficients

$$\mathbf{c}^{obs} = \Pi^{+}\mathbf{P} \in R^{n \times n} \tag{4.5}$$

where $\Pi = \{\psi_1, \psi_2, \cdots, \psi_n\}$ is the pressure modal subspace. A $n$-dimensional quadratic response surface of the form $\mathbf{c}^{obs} = f(G_m^{obs})$ is computed for the pressure modes as a function of the observational mass fluxes, $G_m^{obs}$. The weight coefficients for pressure modes corresponding to the desired mass flow rate $G_m^t$ are then evaluated as $\mathbf{c} = f(G_m^t) = \{c_k\}_{k=1}^r$ and the approximate pressure field is assembled as

$$P^r = \sum_{i=1}^{r} c_i \psi_i \tag{4.6}$$

The energy captured by each POD mode is computed as $E_i = \lambda_i / \sum_{j=1}^{n} \lambda_j$ and the total energy resolved using the first $r$ modes is $E^r = \sum_{i=1}^{r} \lambda_i / \sum_{i=1}^{n} \lambda_i$, where $\lambda_k$ are the eigenvalues of $(\frac{1}{n})U^T U \in R^{n \times n}$ with $U = \mathbf{U}$, $\mathbf{T}(=\{T_1, T_2, \cdots T_n\})$, and $\mathbf{P}$ for velocity, temperature, and pressure observation assembly, respectively.

**4.3 Computational Case Study**

To demonstrate the methodology, consider the example model shown in Figure 4.1. The intake and exhaust plena are symmetrical and both measure 2*L* x 5*L*, with *L* = 0.1 m. The flow straightening duct and server measure *L* x *L*/2 and 4*L* x *L*, respectively, as shown in Figure 4.1(b). All models were developed for the range 72,92 ≤ $Re_L$ ≤ 26,768. Tables 4.1, 4.2 and 4.3 list the observations used to construct the component ROMs. It is noted that the pressure boundary conditions are specified for intake plenum, whose flow is pressure driven. The velocity boundary conditions are specified at the inlet, and pressure boundary conditions at the outlet for both server and exhaust plenum.

To justify the accuracy of POD results, the following Euclidean *L2* error norm is defined

$$V_{err}^r = \frac{||V^r - V^t||}{||V^t||} \tag{4.7}$$

where *V* represents velocity, pressure, and temperature rise over ambient temperature, respectively.

Table 4.1 Intake plenum flow observations, $\Delta P$ [Pa] and $\dot{m}$ [kg/s]

| | Outlet 1 | | Outlet 2 | | Outlet 3 | |
|---|---|---|---|---|---|---|
| $k$ | $\Delta P_1$ | $\dot{m}_1$ | $\Delta P_2$ | $\dot{m}_2$ | $\Delta P_3$ | $\dot{m}_3$ |
| 1 | 1.8 | 0.185 | 11.4 | 0.135 | 12.0 | 0.136 |
| 2 | 3.5 | 0.258 | 22.9 | 0.189 | 23.4 | 0.191 |
| 3 | 5.7 | 0.332 | 37.9 | 0.243 | 38.9 | 0.246 |
| 4 | 8.4 | 0.406 | 57.1 | 0.297 | 57.1 | 0.301 |
| 5 | 11.6 | 0.479 | 78.8 | 0.350 | 81.2 | 0.356 |
| 6 | 15.2 | 0.553 | 104.3 | 0.405 | 109.4 | 0.411 |
| test | 10.4 | 0.461 | 70.9 | 0.337 | 73.8 | 0.342 |

Table 4.2 Server flow observations, $\Delta P$ [Pa], $\dot{m}$ [kg/s] and $Q$ [W]

| | Server 1 | | | Server 2 | | | Server 3 | | |
|---|---|---|---|---|---|---|---|---|---|
| $k$ | $\Delta P_1$ | $\dot{m}_1$ | $Q_1$ | $\Delta P_2$ | $\dot{m}_2$ | $Q_2$ | $\Delta P_3$ | $\dot{m}_3$ | $Q_3$ |
| 1 | 0.54 | 0.185 | 60 | -1.41 | 0.135 | 45 | -0.15 | 0.136 | 50 |
| 2 | 1.10 | 0.258 | 75 | -2.72 | 0.189 | 60 | -0.37 | 0.191 | 65 |
| 3 | 1.83 | 0.332 | 90 | -4.70 | 0.243 | 75 | -0.68 | 0.246 | 80 |
| 4 | 2.67 | 0.406 | 105 | -7.14 | 0.297 | 90 | -1.07 | 0.301 | 95 |
| 5 | 3.65 | 0.479 | 120 | -9.69 | 0.350 | 105 | -1.54 | 0.356 | 110 |
| 6 | 4.80 | 0.553 | 135 | -12.71 | 0.405 | 120 | -2.01 | 0.411 | 125 |
| test | 3.26 | 0.461 | 110 | -9.23 | 0.337 | 110 | -1.42 | 0.342 | 90 |

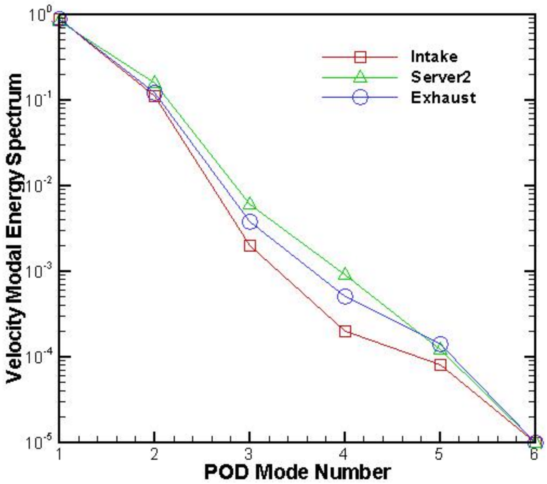
Table 4.3 Exhaust plenum flow observations, $\Delta P$ /Pa and $\dot{m}$ /kg/s

| | Outlet 1 | | Outlet 2 | | Outlet 3 | |
|---|---|---|---|---|---|---|
| $k$ | $\Delta P_1$ | $\dot{m}_1$ | $\Delta P_2$ | $\dot{m}_2$ | $\Delta P_3$ | $\dot{m}_3$ |
| 1 | 16.5 | 0.185 | 14.9 | 0.135 | 13.4 | 0.136 |
| 2 | 32.7 | 0.258 | 29.0 | 0.189 | 26.3 | 0.191 |
| 3 | 53.9 | 0.332 | 48.7 | 0.243 | 43.7 | 0.246 |
| 4 | 80.1 | 0.406 | 73.1 | 0.297 | 65.6 | 0.301 |
| 5 | 112.9 | 0.479 | 102.7 | 0.350 | 91.4 | 0.356 |
| 6 | 150.2 | 0.553 | 136.8 | 0.405 | 121.9 | 0.411 |
| test | 104.8 | 0.461 | 95.2 | 0.337 | 84.6 | 0.342 |

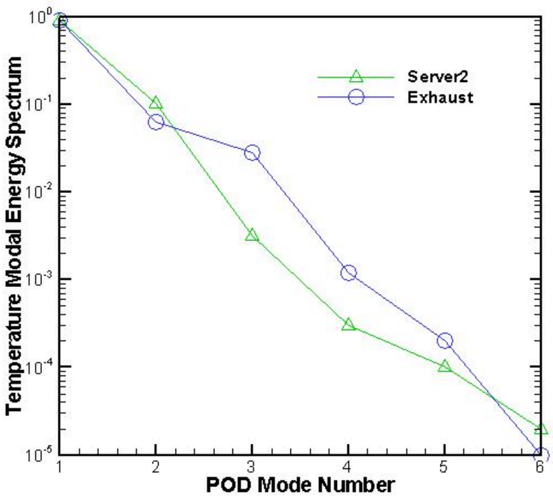
### 4.3.1 Component Level Simulation

The velocity modal spectra for the three models for representative test case shown in Tables 4.1, 4.2 and 4.3 are plotted in Figure 4.8(a), which indicates that the first modes dominate the system energy. It should be noted that the cases k=1~6 in Tables 4.1, 4.2, and 4.3 are used for snapshots and the case $k$=test is for the verification of POD modeling.

The plenum model contained 4,141 grid cells, or 24,846 total DOF to model the flow considering *u, v, P, T, k, ε* are solved for in each grid cell, while the reduced order model contains only 6×3=18 DOF, for an $O(10^3)$ reduction in DOF. Similarly, an $O(10^3)$ reduction in DOF can be achieved for server and exhaust plenum models. The *L2* error norm for the velocity field showed that the boundary conditions were satisfied with 3% and velocity approximation error was 3.5%. Figure 4.9 compares the velocity fields obtained by both CFD and POD simulations for the three sub-domain models. Close agreement is achieved between the true and approximate solutions, both within the field and at the boundary. The approximations of pressure fields for the three ROMs of the example considered are shown in Figure 4.10, which are also in good agreement with the CFD simulations.




(a)




(b)

Figure 4.8 Model spectra for the POD procedure: (a) velocity, (b) temperature

Figure 4.10(b) plots the temperature modal spectra, and Figure 4.11 illustrates the temperature fields for server 2 and exhaust plenum models with POD and CFD, respectively. It is noted that only partial range of temperatures is shown for the server model for improved visualization. Using the first single mode, the POD method has a L2 error norm of less than 7.4% for server2. The largest errors occur near the surface of the blocks where the largest temperature gradients occur. The primary reason that temperature has larger error than the velocity and pressure is that the total heat flow rate, instead of the heat flux at each surface of the heating block is matched. In contrast, fluid flow rate is matched at a single interface such as inlet or outlet, which generates better approximation. Another possible reason is that the error of flow field may propagate to the temperature field. Table 4.4 summarizes the POD modeling errors for each component for representative test case shown in Tables 4.1, 4.2 and 4.3.

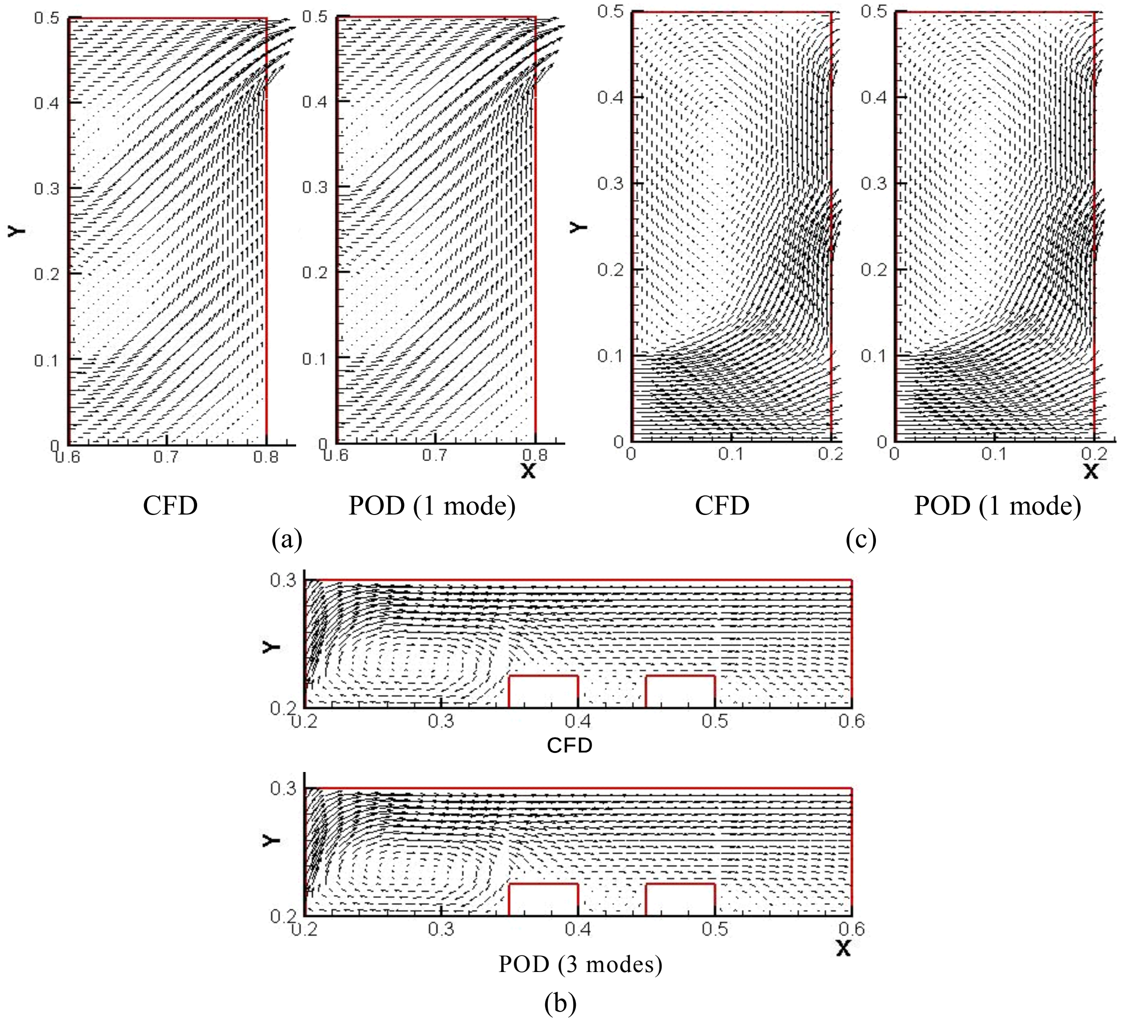



Figure 4.9 Velocity comparison of CFD and POD simulation results: (a) intake plenum, (b) server 2, and (c) exhaust plenum

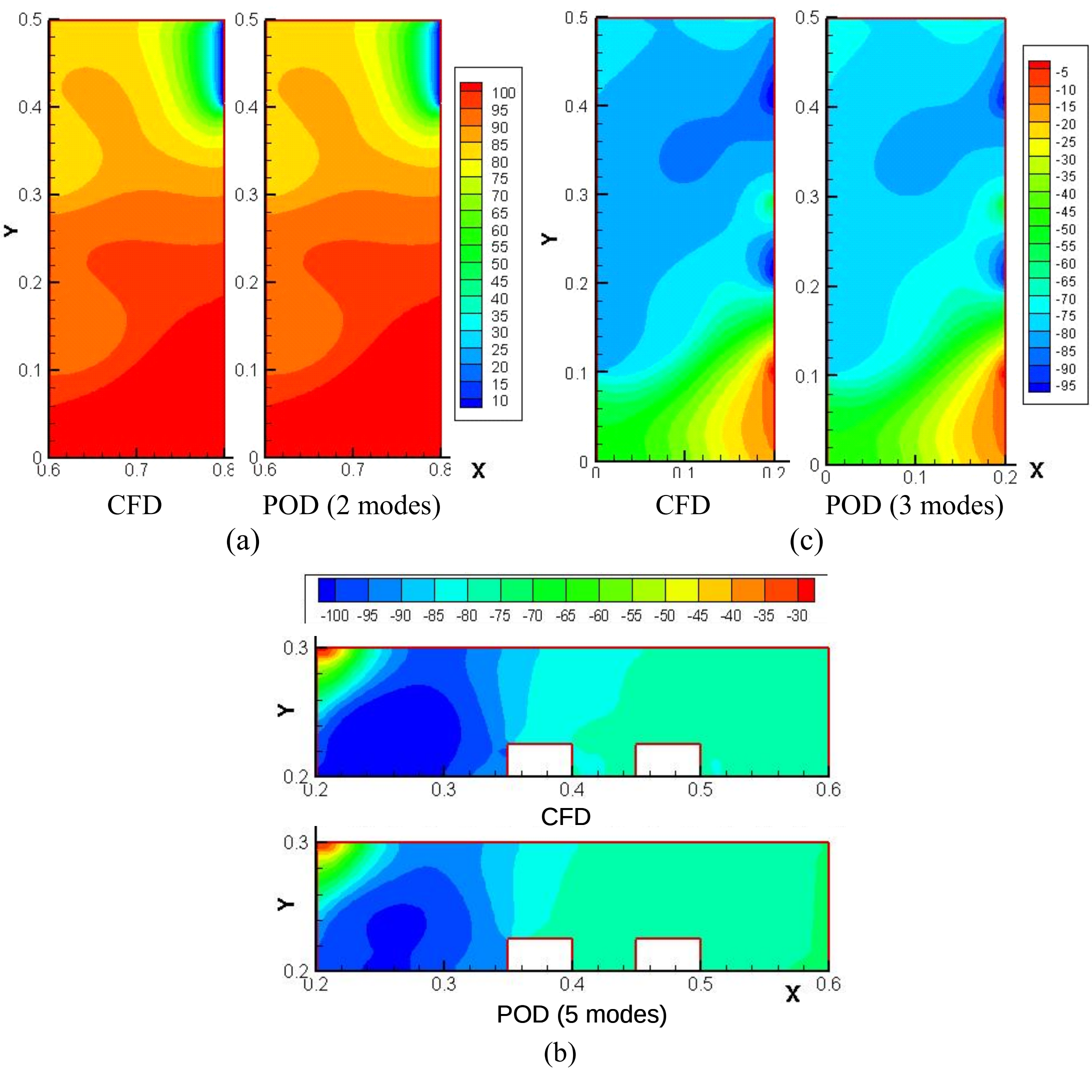
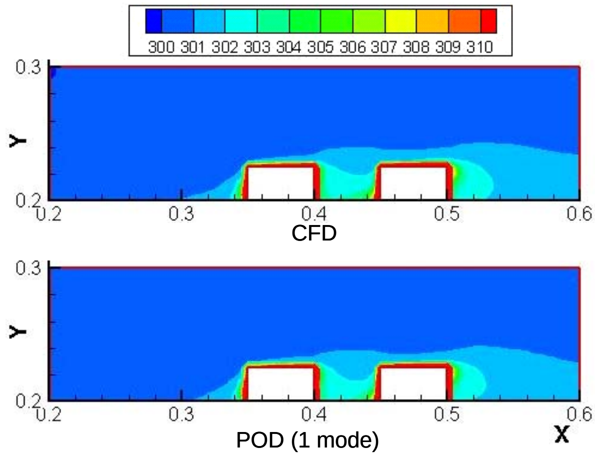


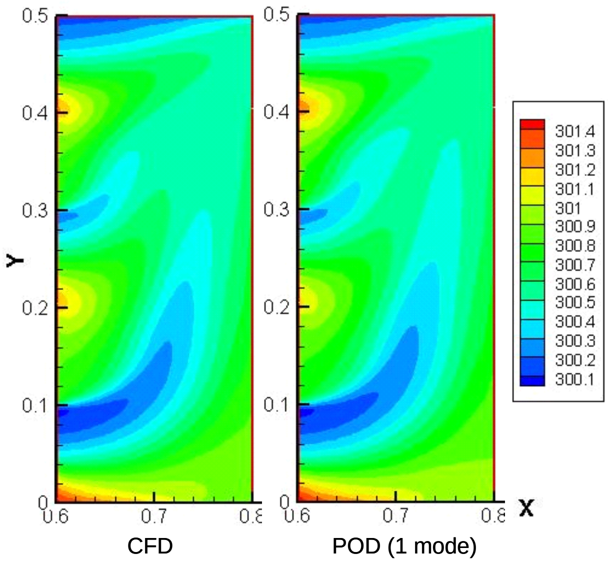

Figure 4.10 Pressure (Pa) comparison of CFD and POD simulation results: (a) intake plenum, (b) server 2, and (c) exhaust plenum

Table 4.4 POD modeling error norm (Error), %, and number of POD modes (#) used

| | Intake | | Server1 | | Server2 | | Server3 | | Exhaust | |
|---|---|---|---|---|---|---|---|---|---|---|
| | # | Error | # | Error | # | Error | # | Error | # | Error |
| Velocity | 1 | 2.1 | 4 | 0.7 | 3 | 0.9 | 1 | 2.5 | 1 | 0.4 |
| Pressure | 2 | 1.3 | 5 | 1.0 | 5 | 3.2 | 5 | 1.2 | 3 | 0.2 |
| Temperature | NA | NA | 1 | 5.6 | 1 | 7.4 | 1 | 7.0 | 1 | 7.2 |




(a)




(b)

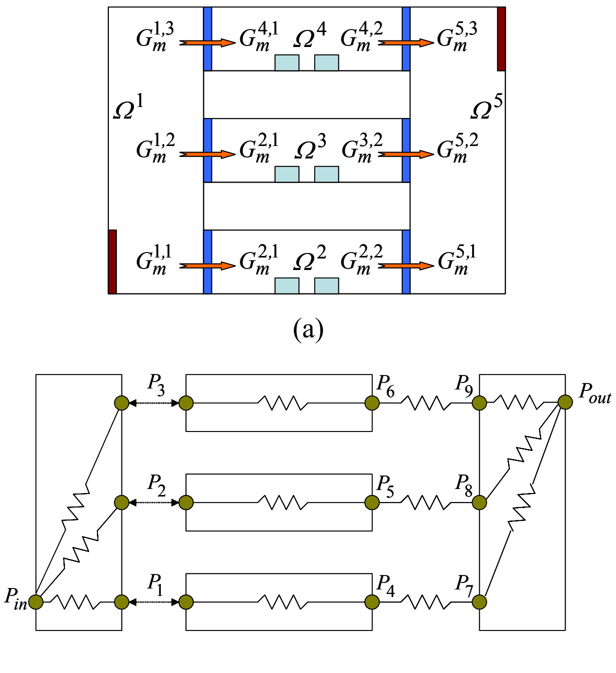
Figure 4.11 Temperature (K) comparison of CFD and POD simulation results: (a) server 2, and (b) exhaust plenum

### 4.3.2 System Level Simulation

The system-level model is constructed by connecting the three server ROMs and the intake and exhaust plena ROMs together. Induced fan models are placed at the outlet of the server models to drive the system flow. The inlet and outlet pressures to the system can be assumed to be zero without loss of generality. A cubic pressure-velocity relationship is used for the fan model

$$\Delta P(u) = 200 - 40u + 20u^2 - 4u^3 \tag{4.8}$$

where the area-averaged velocity $u$ at the horizontal direction is based on the control volumes at the interface. The system nomenclature and flow network are illustrated in Figure 4.12. It is noted that each component sub-domain is identified with a superscript as $\Omega^j$, $j = 1,2,...,5$ and the mass or heat flux at the $k^{th}$ control surface (interface) for the $j^{th}$ sub-domain as $G^{j,k}$. The heat loads for the chips within server 1, server2, and server 3 are 110W, 110W, and 90W, respectively. A zero gauge pressure is set at both inlet and outlet of the cabinet.




(b)

Figure 4.12 FNM: (a) system nomenclature, and (b) system flow resistance network

The pressure loss coefficients $K_1, K_2$ described in Equation (4.2) for each component are summarized in Table 4.5 along with the $r^2$ values (square of correlation coefficient). The pressure drop characteristic of intake and exhaust plena models shown in Table 4.5 may only work for the cases where all connected servers have the same fan settings (many commercial server cabinets indeed have the same fan setting for each server). More snapshots may be needed for more complicated pressure characteristics. The pressure drop characteristics curve of each component is shown in Appendix B.

Table 4.5 Pressure loss coefficients $K_1, K_2$ and $r^2$ for each component

| | Intake | | | Server1 | Server2 | Server3 | Exhaust | | |
|---|---|---|---|---|---|---|---|---|---|
| | Outlet1 | Outlet2 | Outlet3 | | | | Inlet1 | Inlet2 | Inlet3 |
| $K_1$ | 47.256 | 630.89 | 658.52 | 14.857 | -76.43 | -13.33 | 495.25 | 851.77 | 722.52 |
| $K_1$ | 1.507 | 3.995 | -5.951 | 0.531 | -0.872 | 0.48 | -2.324 | -6.132 | 0.038 |
| $r^2$ | 0.99983 | 0.99981 | 0.99884 | 0.99873 | 0.99845 | 0.99237 | 0.99848 | 0.99859 | 0.99951 |

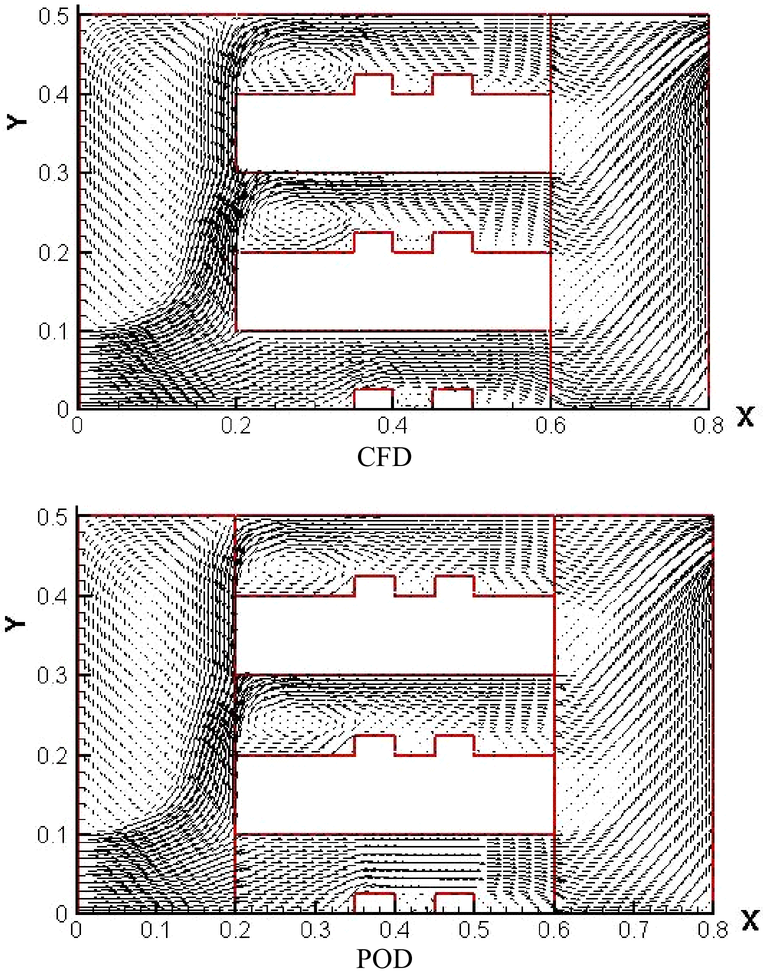


Figure 4.13 Velocity comparison of CFD and POD simulation results at system level

The FNM simulation showed that a relative error for the approximate link mass flow rates over all interfaces was within 4.5% and an error less than 3.9% for nodal pressure over pressure nodes $P_1$ to $P_9$. Figures 4.13, 4.14 and 4.15 plot the full CFD and approximate velocity, pressure and temperature fields, respectively. The FNM-POD simulations show good agreement with CFD simulations and good continuity at the interfaces of sub-domains, which was a problem when no boundary profile is considered. The *L2* error norm is less than 12% for all models, with the largest error occurring at the leading and trailing edges (recirculation regions) of servers and the exhaust plenum. Besides the errors associated with FNM and POD modeling itself, downstream feedback is not captured by this approach. Therefore, this approach may not be valid when strong recirculation occurs inside the system.

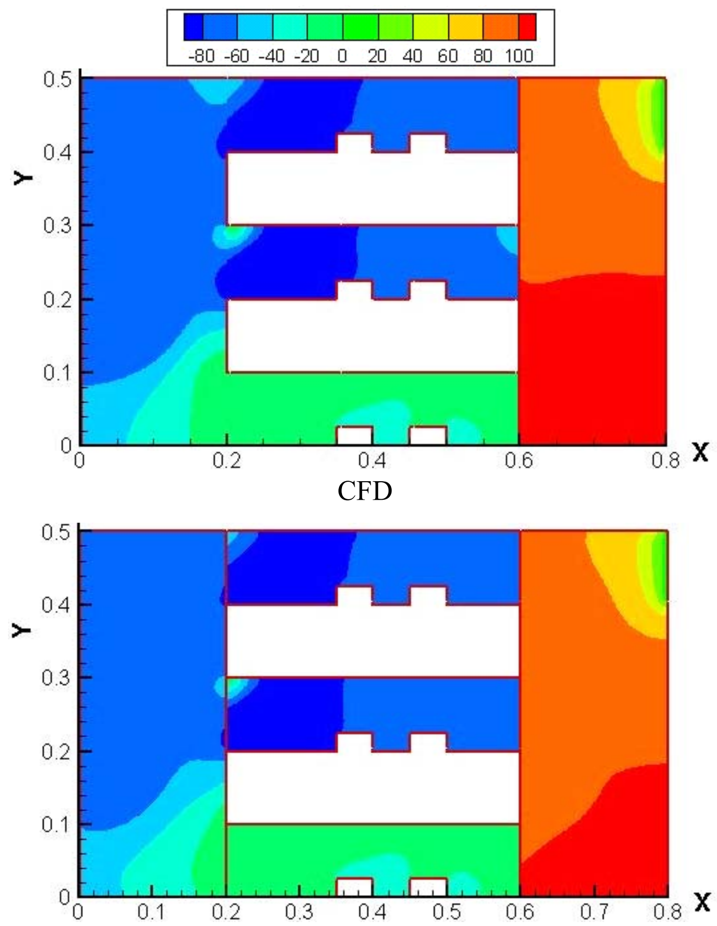



Figure 4.14 Pressure (Pa) comparison of CFD and POD simulation results at system level

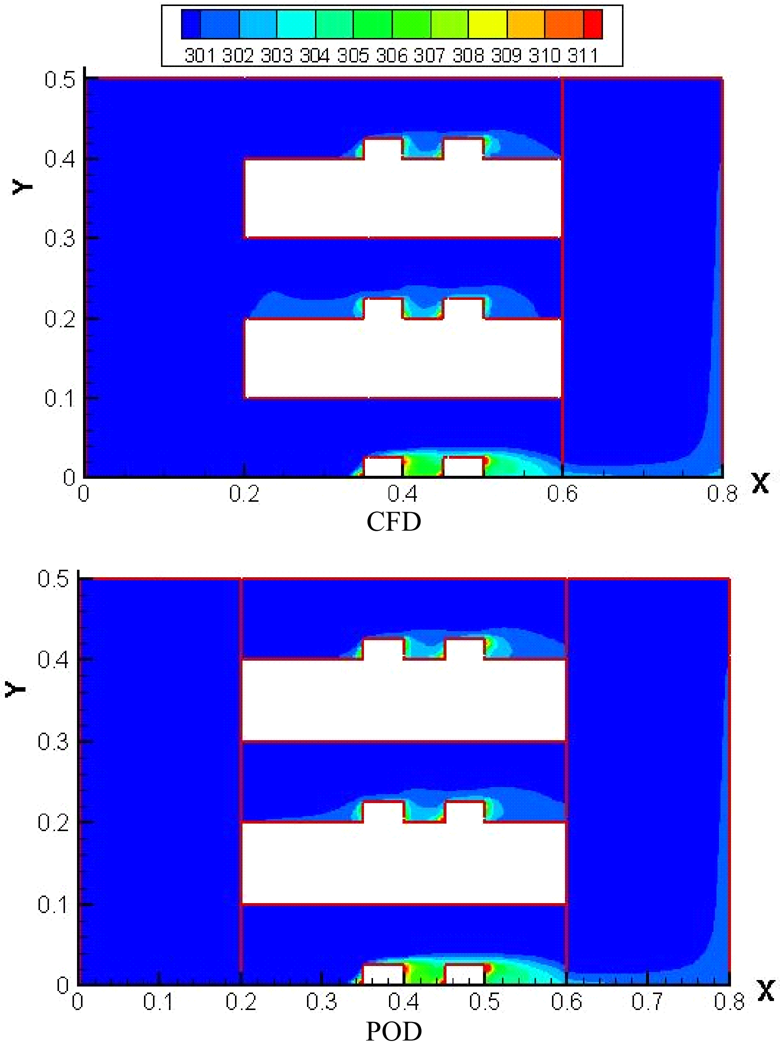
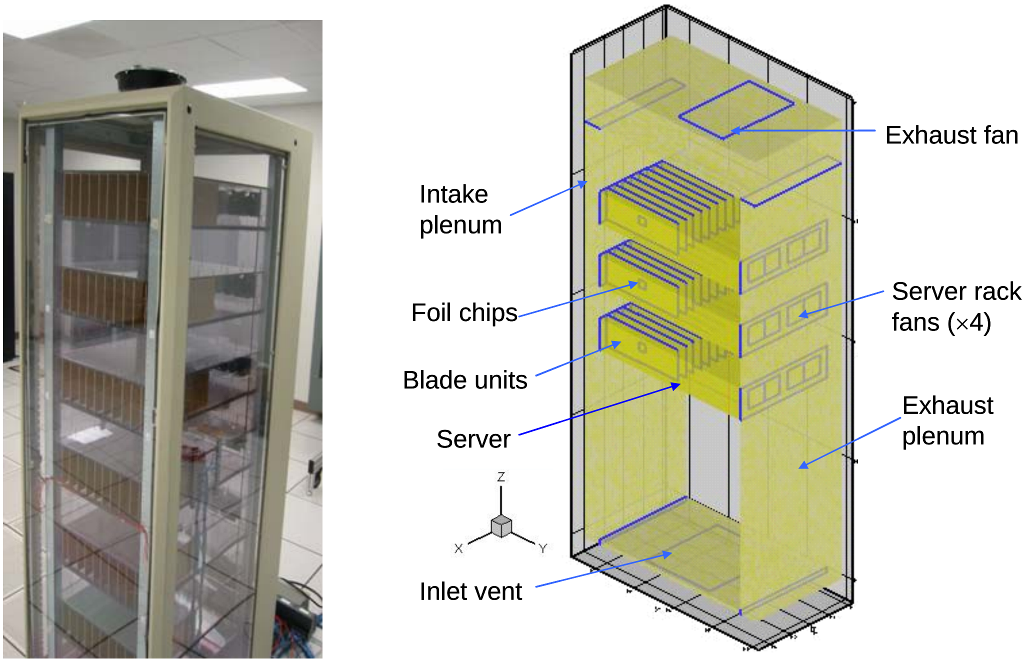



Figure 4.15 Temperature (K) comparison of CFD and POD simulation results at system level

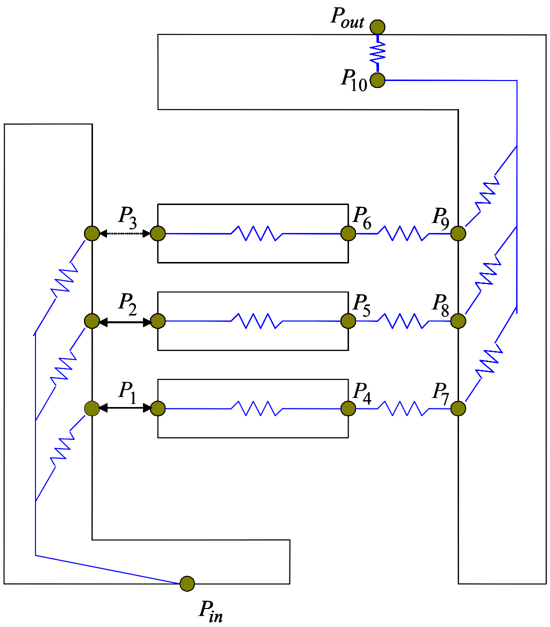
To efficiently capture the downstream effects, an accurate boundary profile needs to be specified downstream, which is typically difficult. Although this profile can be approximated by adding an adjacent component, such as a duct in our case, there is still an error associated with this approximation. These errors contribute to the existing mismatch at the interfaces. The large error in the leading and trailing edges, where the recirculation occurs, of servers will not affect the high heat flux regions (i.e. the chips) significantly since the velocities in those regions are relatively small and the general flow pattern across high heat flux regions is captured by this method. A much smaller error of 7% for the chip maximum temperatures has been achieved with this FNM-POD modeling approach. Another concern in connecting component models is the propagation of error and the accumulation of errors as more components are added to the system. Generally, the connection of components in parallel may not accumulate the modeling errors, but a connection in series may do. However, FNM-POD based ROMs may limit the accumulation of this error because the individual models satisfy overall mass and energy balances. As illustrated earlier, an $O(10^3)$ reduction in DOF was achieved for each ROM, then the system ROM has an $O(10^3)$ reduction in DOF.

### 4.4 Experimental Validation

The system studied in this investigation is a simulated blade server cabinet, whose schematic is shown in Figure 4.16(a) [6]. This server cabinet is cooled using vertically oriented air flow distributed to seven servers with each server containing 10 blade units. Alternating server spaces are filled with blank units to block the airflow. For the demonstration, only servers 4, 5 and 6 are tested in both the numerical modeling and experiments. The complete cabinet measures 0.6 m wide by 0.8 m deep by 2 m tall. Other geometric features and thermal properties are shown in Table 4.6. The overall flow through the cabinet is provided by a maximum of 0.108 $m^3/s$ (550 CFM) exhaust fan on the top of the cabinet and flow movement through the server racks is provided by four 0.015 $m^3/s$ (20 CFM) maximum fans. The blade servers are represented by the channels formed using large pieces of printed wiring board with a foil heater in the center on one side simulating the chip as dividers. Only half of the heaters in servers 4 and 5 are turned on for the testing and modeling. The entire rack is divided into three parts: intake plenum, servers, and exhaust plenum as shown in Figure 4.16(b), and its corresponding flow network is shown in Figure 4.16(c).




(a) (b)



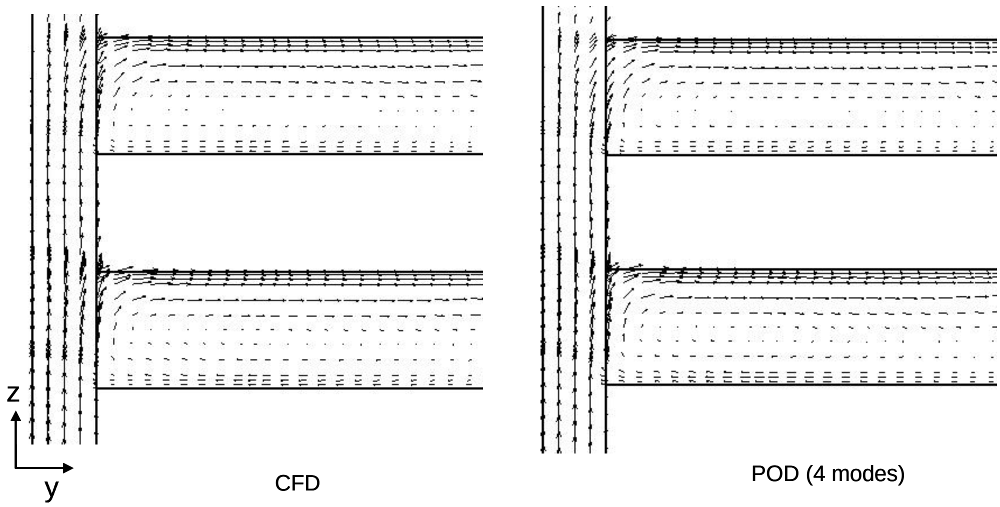

(c)

Figure 4.16 Simulated rack: (a) experimental model, (b) numerical model, and (c) system flow resistance network

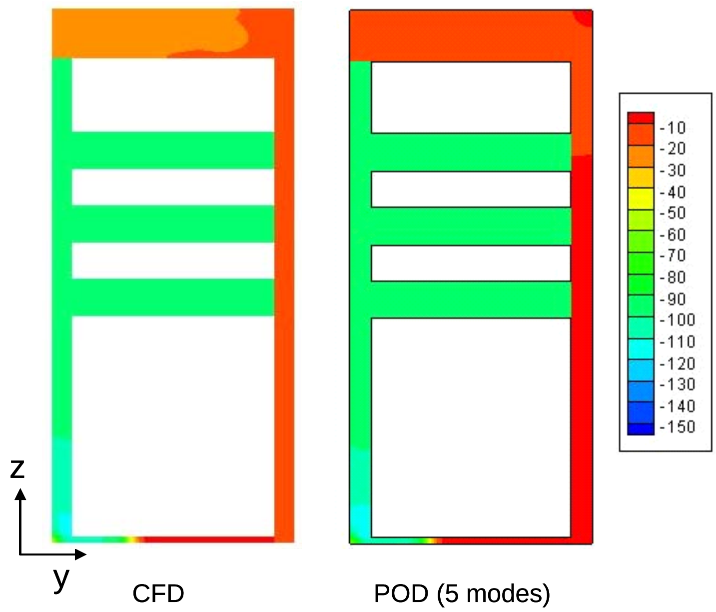
Table 4.6 Simulated rack geometry and properties

| | | |
|---|---|---|
| Blade server unit length | 0.44 | [m] |
| Blade server unit gap | 0.4 | [m] |
| Bottom bay height | 0.20 | [m] |
| Foil chip size | 0.32×0.32 | [m] × [m] |
| Plenum depth | 0.072 | [m] |
| Rack depth | 0.864 | [m] |
| Rack height | 2.00 | [m] |
| Rack width | 0.512 | [m] |
| Rack inlet width | 0.36 | [m] |
| Rack inlet length | 0.32 | [m] |
| Rack exit bay | 0.182 | [m] |
| Rack exhaust fan diameter | 0.15 | [m] |
| Server width | 0.44 | [m] |
| Server depth | 0.72 | [m] |
| Server height | 0.132 | [m] |
| Foil chip thermal conductivity | 387.6 | [W/m-K] |
| FR4 PCB thermal conductivity [2]<br>In plane<br>Lateral | <br>0.204<br>9.074 | [W/m-K] |

The CFD and FNM-POD simulation results for velocity and pressure fields are shown in Figure 4.17 and the results for temperature distributions across the chips and printed wiring board substrates of server 4 ($Q$=10W) and server 5 ($Q$=15W) are shown in Figure 4.18. The CFD and FNM-POD simulations are compared with experiments for chip junction temperature rise over ambient temperature (293K at a data center lab) in Figure 4.19. The FNM-POD simulation results are seen close to the CFD simulation results, with a maximum relative error of 7.9%. Compared to the maximum error up to 15% in some regions (leading and trailing edges of server and exhaust models), the high heat flux regions (i.e. the chip areas) are more accurately predicted at the system level. The FNM-POD results are generally higher than the CFD results. One possible reason is that the duct attached to the intake model for the intake ROM development may not be long enough to fully transmit the flow across the connected server. A larger flow rate may go through the top region of servers, resulting lower convection heat transfer at the chips, compared to the full CFD system level simulation. It can be seen that both FNM-POD and CFD results under-predict the chip junction temperatures with a maximum approximation error of 10%. This is because the real system flow resistance is higher than the numerical model due to the wiring and surface roughness. The contact thermal resistances between chips and thermocouples may also contribute to this discrepancy. The experimental uncertainty of was estimated to be about $\pm 1.2K$, which includes $\pm 0.4K$ for the T-type thermocouples and $\pm 0.8K$ for location and thermal resistance and power supply uncertainties [82]. The system model contained 336,048 grid cells, or 23,252,336 total DOFs to model the flow considering $u, v, w, P, T, k, \varepsilon$ are solved for in each grid cell, while the reduced order model has only 108 DOFs (2×9=18 for flow resistance network, and a maximum of 6×3×5=90 for POD), an $O(10^5)$ reduction in DOF is achieved.

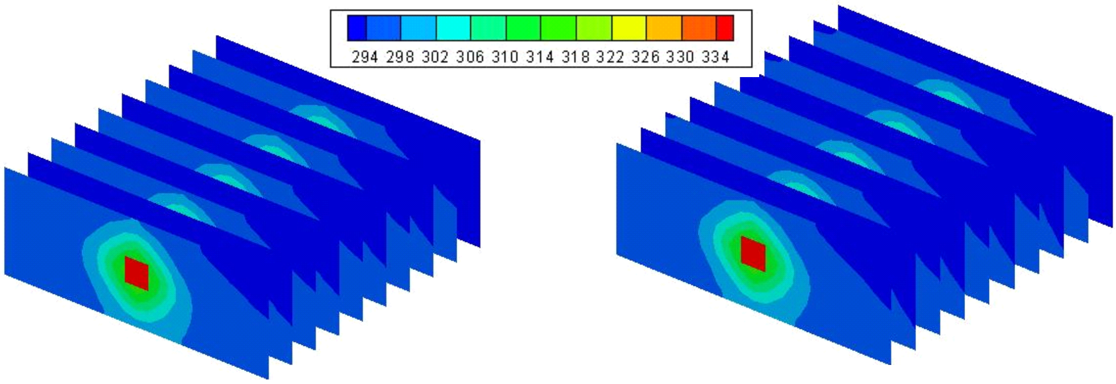



(a)

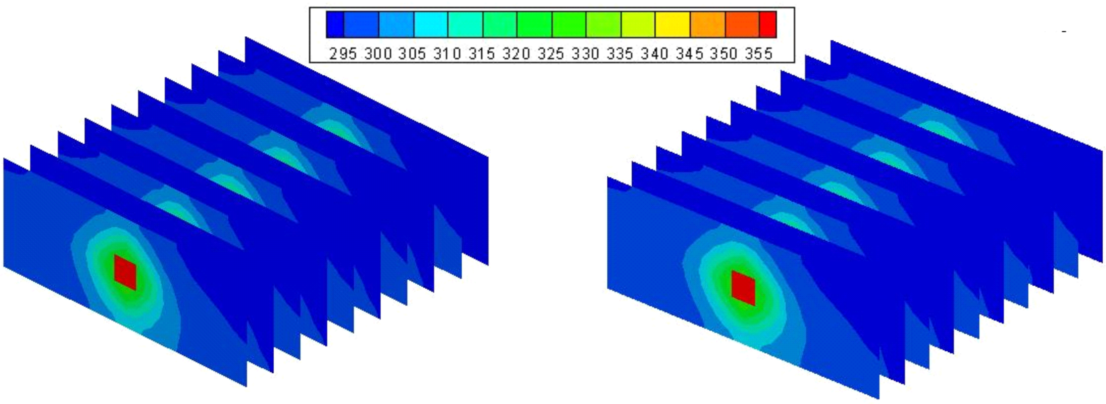



(b)

Figure 4.17 Comparison of CFD and FNM-POD simulation results at system level for simulated rack: (a) velocity field, and (b) pressure field (Pa)

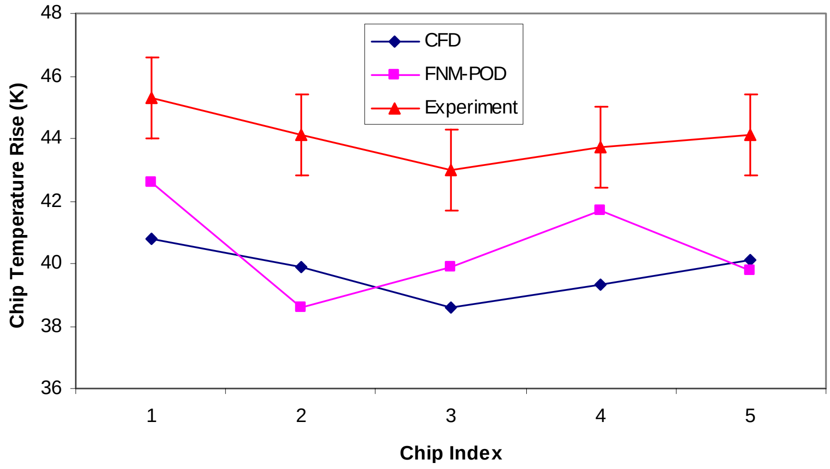



(a)

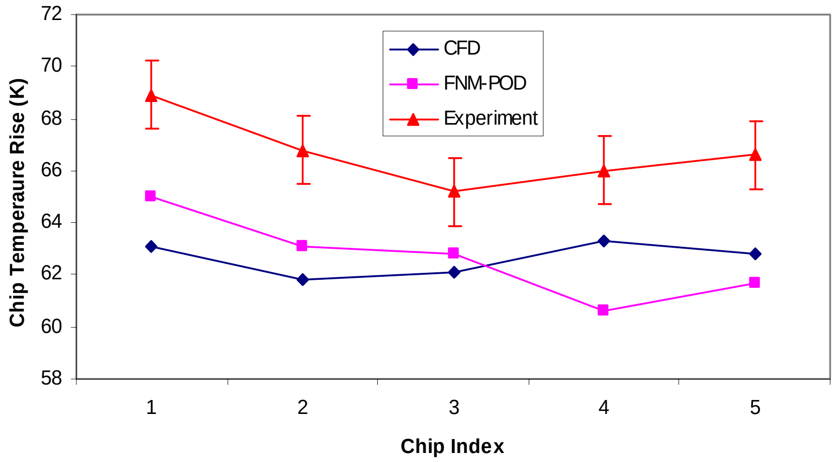



(b)

Figure 4.18 Comparison of CFD and FNM-POD simulation results for temperature distribution across chips and FR4 board at system level for simulated rack: (a) server4, and (b) server5




(a)




(b)

Figure 4.19 Chip junction excess temperature comparison of CFD simulation, POD simulation, and measurement results at system level for mock rack (K): (a) server4, and (b) server5

# CHAPTER 5

# TRANSIENT REDUCED ORDER MODELING

In addition to steady state performance, a number of transient scenarios are of great interest in naval applications such as thermal management of advanced power electronics cabinets [83]. These include transient coupled electro-thermal responses of power electronics and power conversion devices under various operating scenarios, as well as potential failure of a cooling system [83]. A transient reduced order modeling approach is proposed for thermal analysis of electronic systems from the component to the system level. Compact modeling is utilized at component level simulation, and a combination of reduced order modeling and compact modeling is used to conduct the system level simulation.

## 5.1 Model Problem

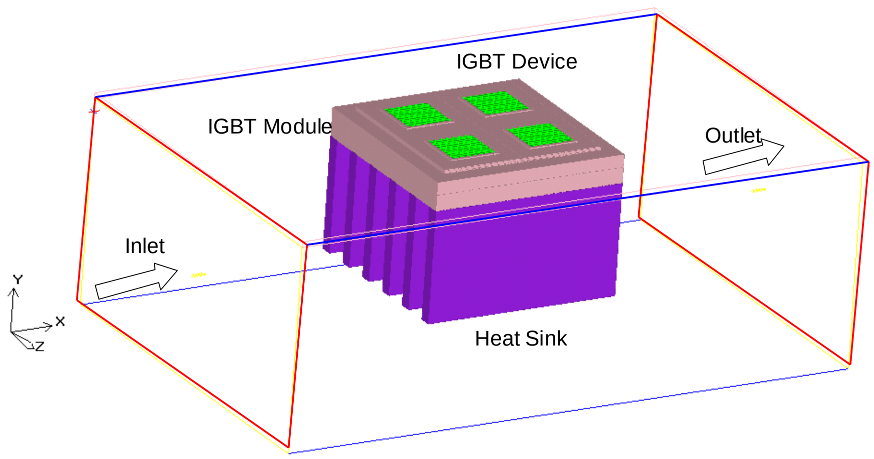



Figure 5.1 Schematic of electronic enclosure with IGBT module

The system selected to illustrate the above approach is an electronic enclosure with an IGBT power module attached to a heat sink, as shown in Figure 5.1. The air enters the system and flow across the heat sink to remove the heat from the IGBT power module, and finally exits the enclosure. The power module consists of four IGBT devices attached to the metallized ceramic substrate (Aluminum Nitride (AlN)) using direct copper bonding (DCB) technology. These ceramic substrates provide electrical insulation to the underlying base plate. Figure 5.2 shows a section across the thickness of an IGBT device. A thin film of copper is applied to the top and bottom surface of the ceramic substrate for good thermal conductivity, and the substrate is attached to the baseplate through solder. The geometry of the system and IGBT module are shown in Table 5.1. The goal of this work is to develop a reduced order modeling methodology for the thermal modeling of this system from the device level to the system level.

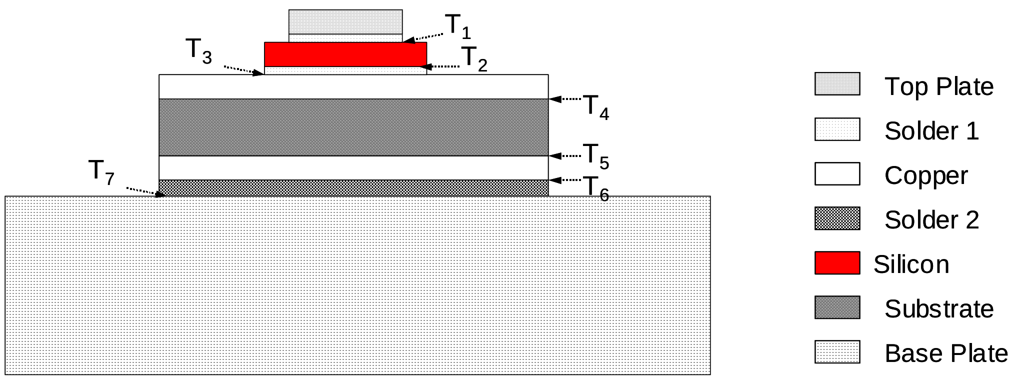



Figure 5.2 Section of IGBT module

Table 5.1 Geometry of enclosure and IGBT module

| | Enclosure | Heat Sink | IGBT |
|---|---|---|---|
| W (mm) | 186 | 62 | 62 |
| D (mm) | 122 | 62 | 62 |
| H (mm) | 65.84 | 40 | 5.78 |

## 5.2 Heat Diffusion Equation

The transient heat flow through a one-dimensional region is characterized by the heat diffusion equation [84]

$$A\rho c_p \frac{\partial T}{\partial t} = A\kappa \frac{\partial^2 T}{\partial z^2} \tag{5.1}$$

A temperature gradient exists across a finite element *z*. *A* represents the area perpendicular to heat flow, and ρ is the density of the material. κ and $c_p$ represent the thermal conductivity and specific heat of the material, respectively. By discretizing the domain as shown in Figure 5.3, the heat diffusion equation can be discretized into a finite number of first order ordinary time-dependent differential equations given by Equation (5.2).

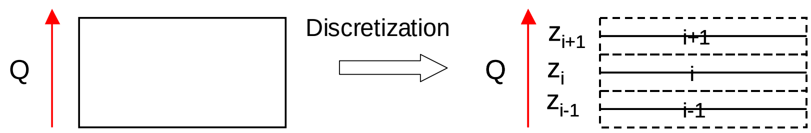



Figure 5.3 Discretization of heat transfer domain and heat diffusion equation

$$\frac{T_{i+1}-T_i}{R_{t,i}} - \frac{T_i - T_{i-1}}{R_{t,i-1}} = \frac{dH_i}{dt} \tag{5.2}$$

where $R_{t,i} = \frac{z_{i+1}-z_i}{A\kappa_{i,i+1}}$, $H_i = C_i \cdot T_i$, and $C_i = A\rho c_p (\frac{z_{i+1}-z_i}{2})$ are called thermal resistance, enthalpy, and capacitance of the finite element or volume *i*, respectively. Equation (5.2) has the same structure as a simulator for a simple R-C circuit with voltages and currents at an electrical node defined by

$$\frac{V_{i+1}-V_i}{R_i} - \frac{V_i - V_{i-1}}{R_{i-1}} = \frac{dC_i V_i}{dt} \tag{5.3}$$

where *V*, *R*, and *C* are the voltage, electric resistance, and electric capacitance of electric node *i*. Therefore, the solution to the R-C electrical circuit will be the same as the solution to Equation (5.2). In other words, a transient thermal resistance network will have the same structure as a R-C circuit with a representative two electrical nodes in series, as shown in Figure 5.4.

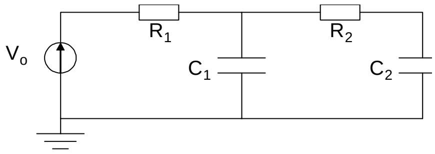



Figure 5.4 Series R-C circuit

Thermal resistance networks have been widely studied for the analysis of electronic packages under both steady state and transient scenarios [27, 85-87], due to their simplicity and often acceptable accuracy. However, such network is difficult to incorporate into system level simulation. An approach to accomplish this is proposed in this chapter.

## 5.3 Component Level Simulation

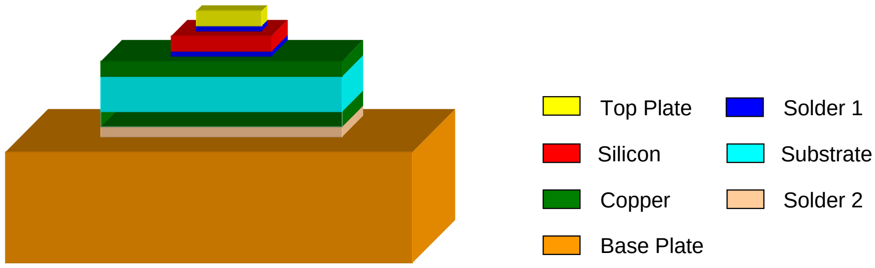



Figure 5.5 Schematic of IGBT component

To conduct the thermal modeling at the component level, one quarter of the IGBT module is considered, as shown in Figure 5.5. A uniform heat source is introduced at the interface between the top solder layer and the silicon. The bottom of the base plate is assumed at a uniform temperature. Since the majority of the heat will be removed through baseplate attached to the heat sink, the top surface and side surfaces of the IGBT device are assumed adiabatic. Also, the top plate and the top solder layer between the top plate and silicon are omitted without loss generality due to adiabatic boundary condition at the top surface. The geometry of this model is shown in Table 5.2, and the thermal properties of materials are shown in Table 5.3.

Table 5.2 Geometry of IGBT device

| | Silicon | Solder1 | Copper | Substrate | Solder2 | Base Plate |
|---|---|---|---|---|---|---|
| W (mm) | 16 | 16 | 26 | 26 | 26 | 34 |
| D (mm) | 16 | 16 | 26 | 26 | 26 | 34 |
| t (mm) | 0.4 | 0.05 | 0.3 | 0.65 | 0.08 | 4 |

Table 5.3 Thermal properties of IGBT device materials [88]

| Material | Silicon | Copper | Substrate | Solder | Base Plate |
|---|---|---|---|---|---|
| $\rho$ (Kg/m$^3$) | 2,320 | 8,960 | 3,260 | 7,400 | 2,980 |
| $\kappa$ (W/m-K) | 148 | 393 | 170 | 40 | 180 |
| $C_p$ (J/Kg-K) | 700 | 276 | 669 | 160 | 722 |

### 5.3.1 Detailed simulation

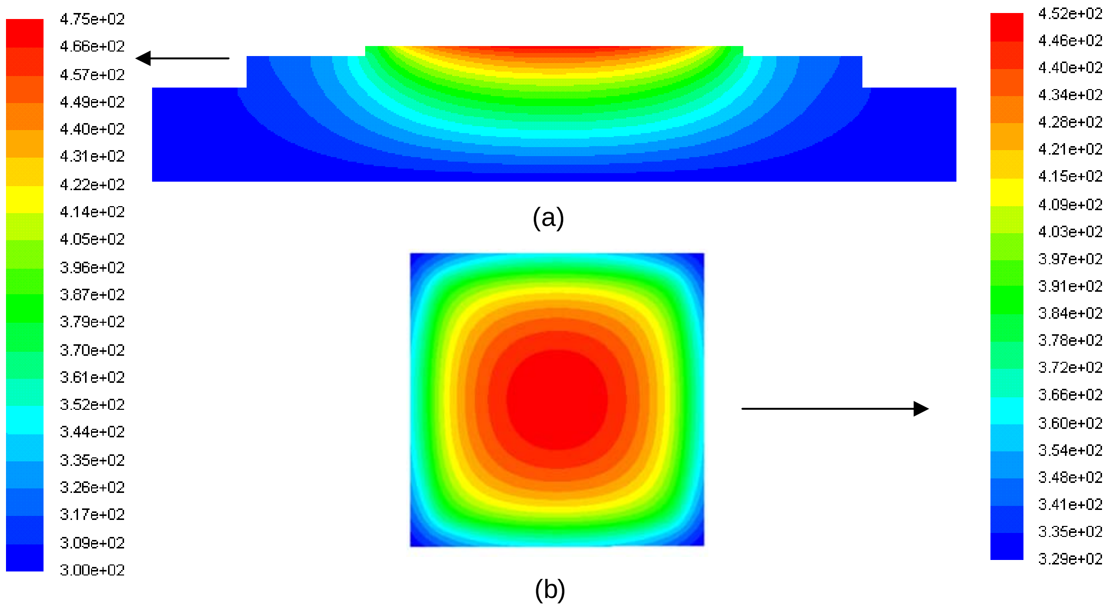



Figure 5.6 Temperature contour (K), (a) section of device, (b) $T_2$ surface

A detailed numerical model has been developed for this IGBT device with a mesh size of 231,398. The temperature contours at the section of IGBT device and at the $T_2$ surface shown in Figure 5.2 under steady state are depicted in Figure 5.6. The temperature rise over ambient (300K) at each interface defined in Figure 5.2 with time is depicted in Figure 5.7. It can be seen that the system reaches the steady state after about 0.6 seconds. A time step of 0.01 with 100 steps was used during the transient simulation.

The total computation time is about 20 minutes. It is noted that the contact thermal resistance at each interface is neglected.

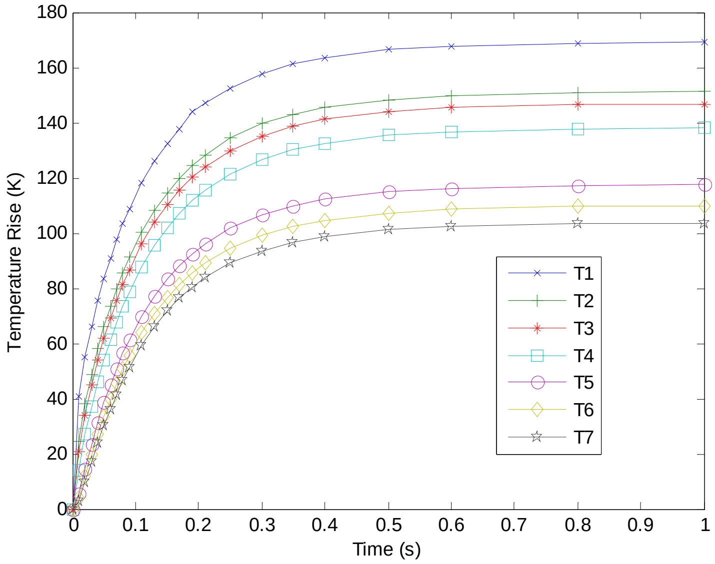



Figure 5.7 Temperature rise at each interface obtained by detailed simulation

### 5.3.2 Compact modeling

It can be seen that the smallest length scale of the detailed model described in previous section is only 50 μm, which results in a large mesh size for the IGBT model and therefore system model. A compact model is necessary to eliminate the small length scales. Although thermal resistance network can significantly simplify the problem, it is very difficult to incorporate into system level simulation. As described in Chapter 2, a multi-layer compact model can be accurate and efficient to incorporate into system level simulations. A general approach to develop multi-layer transient compact model for IGBT device and therefore IGBT module through resistance network is proposed here, as shown in Figure 5.8. The first step is to collect the geometry information and thermal properties of the original numerical model. Then the detailed numerical simulation is conducted, and necessary thermal information from the numerical simulation is extracted.

A thermal resistance network for the numerical model is then constructed based on the extracted thermal information. The solution to the thermal resistance network is then obtained via a dedicated numerical solver or commercial software such as SPICE. A simplified thermal resistance network can be obtained by analyzing the solution to the original thermal resistance network. A multi-layer model is then constructed by reforming the geometry and thermal properties based on the simplified thermal resistance network. As the final step, numerical modeling is conducted for the multi-layer compact model, and the simulation results are compared to that of original detailed model.

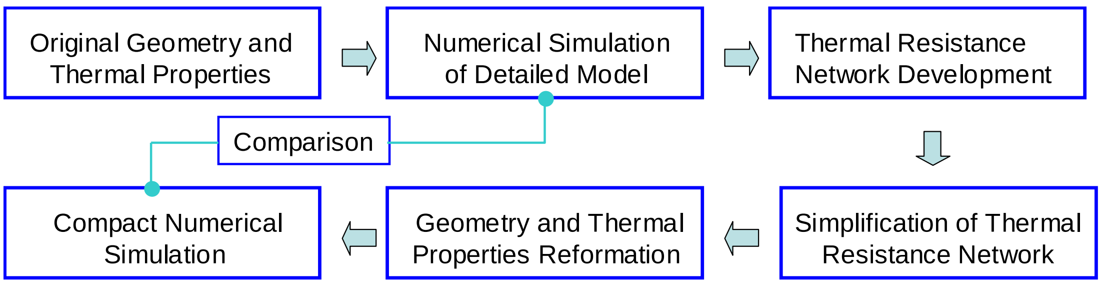



Figure 5.8 Approach of transient compact modeling

**(1) Thermal resistance network development**

To apply this approach for the development of a multi-layer compact model for the transient simulation of the IGBT device under investigation, a thermal resistance network for the IGBT device model based on the detailed numerical simulation needs to be developed. Since the device has seven layers, a thermal resistance network with seven thermal resistors and capacitors is constructed for the IGBT device model, as shown in Figure 5.9. Q is the heat source (1200 W) and $T_0$ is the temperature (300 K) of the bottom surface of the base plate. $T_1$ to $T_7$ are defined in Figure 5.2. It is noted that more resistors and capacitors may be needed if materials with lower thermal conductivity exist.

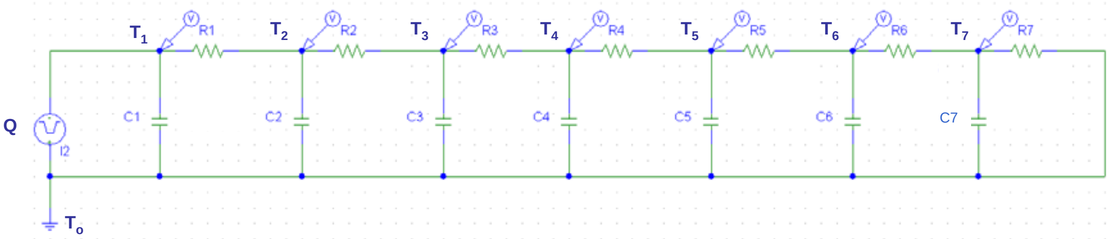


Figure 5.9 Thermal resistance network of the IGBT device

The next step is to calculate the thermal resistance and capacitance of each layer. Thermal resistances of electronic package can be generally divided into two parts. The first is the 1-D resistance, and the other is spreading resistance, as described by

$$R_t = R_f + R_{sp}, \text{ where } R_f = t/(\kappa \cdot A) \tag{5.4}$$

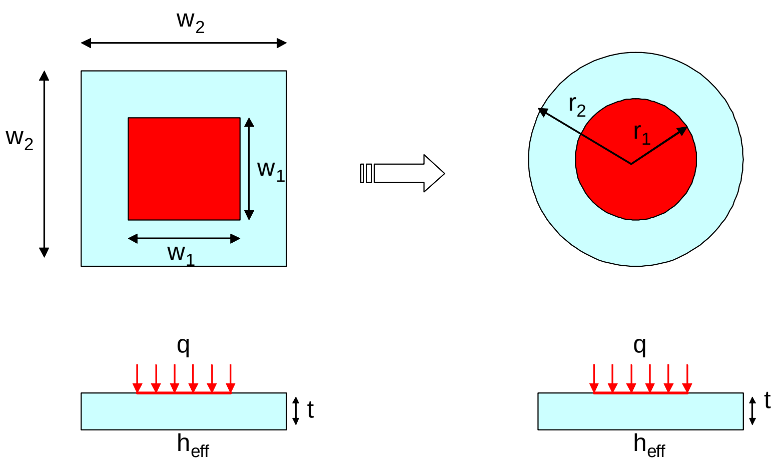


Figure 5.10 Transformation of a square spreader and heat source into circular geometry [90]

The spreading resistance $R_{sp}$ exists when the heat source area is smaller than the substrate area. It is important to find an accurate and efficient way to characterize the spreading resistance for chip packages due to its dominance in many cases. There have been a number of theoretical and experimental studies to estimate spreading resistance [84, 89]. Relatively simpler solutions have been provided by Lee *et. al*. [88], that yield solutions close to those of analytical solutions and can be easily programmed. The solution is based on a circular spreader plate and circular heat source. Square spreader plate and heat source can be converted to circular geometry as shown in Figure 5.10. The transformation is based on the areas of the plate and heat source being the same for both the square and circular geometries. Therefore, the equivalent radii in the circular case are given by

$$r_1 = \sqrt{W_1^2 / \pi} \text{ and } r_2 = \sqrt{W_2^2 / \pi} \tag{5.5}$$

With the radii and thermal conductivity κ and thickness *t* of the spreader plate, the spreading resistance can be calculated by

$$R_{sp} = \frac{\psi_{\max}}{\kappa \cdot r_1 \cdot \sqrt{\pi}} \tag{5.6}$$

where the terms are defined by $\psi_{\max} = \dfrac{\varepsilon \cdot \pi}{\sqrt{\pi}} + \dfrac{1}{\sqrt{\pi}(1-\varepsilon)\Phi}$, $\Phi = \dfrac{\tanh(\lambda \cdot \eta) + \lambda / Bi}{1 + \dfrac{\lambda}{Bi}\tanh(\lambda \cdot \eta)}$,

$\lambda = \pi + \dfrac{1}{\varepsilon\sqrt{\pi}}$, $Bi = \dfrac{h_{eff} r_2}{\kappa}$, $\eta = \dfrac{t}{r_2}$ and $\varepsilon = r_1 / r_2$. $h_{eff}$ is the effective heat transfer coefficient imposed on the other surface the plate. The formula has been proven to be accurate within a certain range of the dimension of the spreader [91]. However, this method may not be valid when large differences exist between the sizes of spreader and heat source. The actual spreading distance of the heat depends on the size of the heat source, the properties of the spreader and the boundary conditions. Therefore, it is very important to find an actual spreading distance for the spreader. The heat is assumed to spread from the bottom of the IGBT device downward through the package at a 45 degree angle in [92]. This is an empirical estimation of the actual spreading dimension for a particular IGBT device. A general approach to estimate the spreading distance of any package is proposed here. Numerical simulation is conducted on the package at first, the total thermal resistance of each material is then calculated by

$$R_t = \frac{\Delta T}{Q} \tag{5.7}$$

where Q is the heat dissipation, and ΔT is the temperature gradient across the material. With the calculated total thermal resistance for each layer, the actual spreading dimension ($r_2$) can be obtained through Equations (5.4) and (5.6). The calculation starts from the silicon layer, where the heat source dimension $r_1$ is known, and goes through the package. With the calculated spreading dimension, the heat capacitance can be obtained by

$$C_i = \rho c_p V_i \tag{5.8}$$

where the volume $V_i$ of layer $i$ is calculated from a cone with $r_i$ and $r_{i+1}$ as the top and bottom radius respectively, as shown in Figure 5.11. The calculated thermal capacitance and total thermal resistance of each layer is shown in Table 5.3. The corresponding thermal time constants $\tau = R \cdot C$ are also shown in the same table.

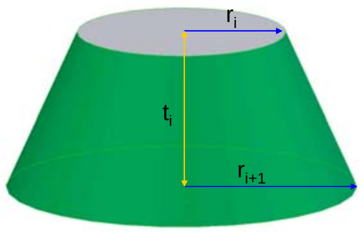



Figure 5.11 Schematic of volume $V_i$

With these capacitance and resistance, the solution to the thermal resistance network shown in Figure 5.9 can be solved with SPICE. Figure 5.12 shows the temperature rise over ambient (300 K) with time at each surface defined in Figure 5.4. It can be seen that the results are very close to that achieved by detailed numerical simulation as shown in Figure 5.7.

Table 5.4 Thermal capacitance and thermal resistance of layers

| | Silicon | Solder1 | Copper1 | Substrate | Copper2 | Solder2 | Base Plate |
|---|---|---|---|---|---|---|---|
| R (K/W) | 0.0151 | 0.00373 | 0.0072 | 0.0171 | 0.0064 | 0.00435 | 0.0865 |
| C (J/K) | 0.03 | 0.0037 | 0.0481 | 0.1025 | 0.0595 | 0.0079 | 1.210 |
| $\tau$ (ms) | 0.453 | 0.0138 | 0.3463 | 1.7528 | 0.3808 | 0.0344 | 104.665 |

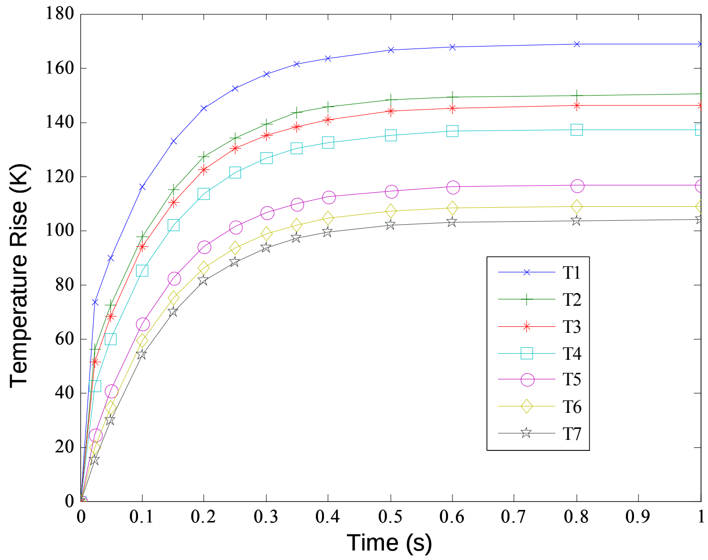



Figure 5.12 Temperature rise at each interface

**(2) Simplification of thermal resistance network**

An examination of Table 5.3 tells that the thermal time constants of silicon, substrate, and base plate are much larger than that of other layers. This means the thermal resistance network shown in Figure 5.9 can be simplified by combining several thermal resistors and capacitors together. Considering silicon and solder layer 1 have the same width, their resistors and capacitors can be merged together. Similarly, the resistors and capacitors of copper, substrate and solder layer 2 can be merged together. The model after merging materials is shown in Figure 5.13, with $T_1$, $T_3$, and $T_7$ being the temperatures at the same interfaces as those shown in Figure 5.2. Figure 5.14 shows the simplified thermal resistance network with corresponding values of resistance and capacitance for each new material.

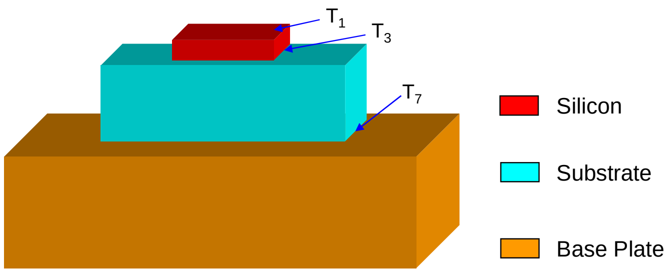



Figure 5.13 Simplified model of IGBT device

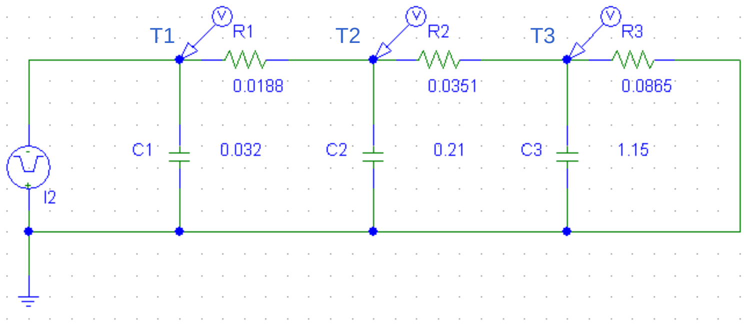



Figure 5.14 Simplified thermal resistance network

The corresponding temperature rise at $T_1$, $T_3$, and $T_7$ are shown in Figure 5.15, which indicates that the results are very close that for $T_1$, $T_3$, and $T_7$ shown in Figures 5.7 and 5.12. This proves that the simplification of thermal resistance network is successful.

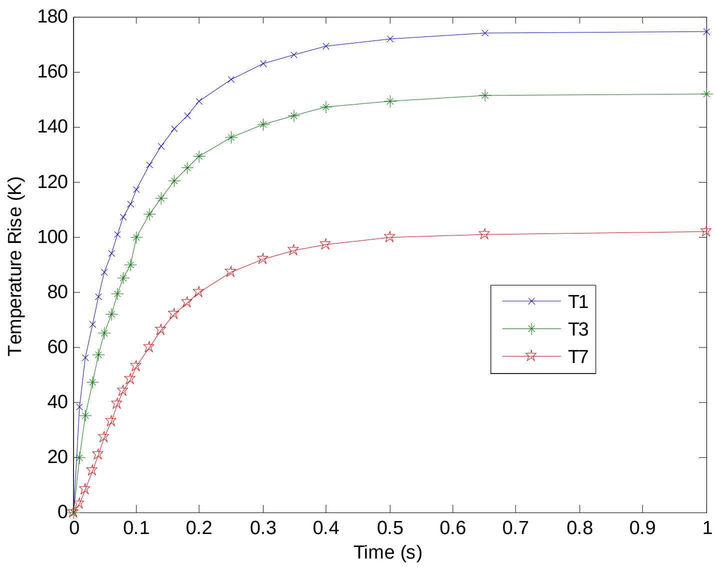



Figure 5.15 Temperature rise through simplified thermal resistance network

**(3) Development of multi-layer compact model**

With the simplified thermal resistance network as shown in Figure 5.14, the corresponding multi-layer compact model is shown in Figure 5.13. The key point of this compact model is to find the effective thermal properties for each layer. Given the thermal resistances and capacitances and the same spreading dimensions as detailed model, the thermal properties can be traced back via Equations (5.4) to (5.8), as shown in Table 5.5.

Table 5.5 Temperature rise through simplified thermal resistance network

| Material | Silicon | Substrate | Base Plate |
|---|---|---|---|
| $\rho$ (Kg/m$^3$) | 2,320 | 3,260 | 2,980 |
| $\kappa$ (W/m-K) | 130.4 | 196.31 | 180 |
| $C_p$ (J/Kg-K) | 474.4 | 481.83 | 722 |

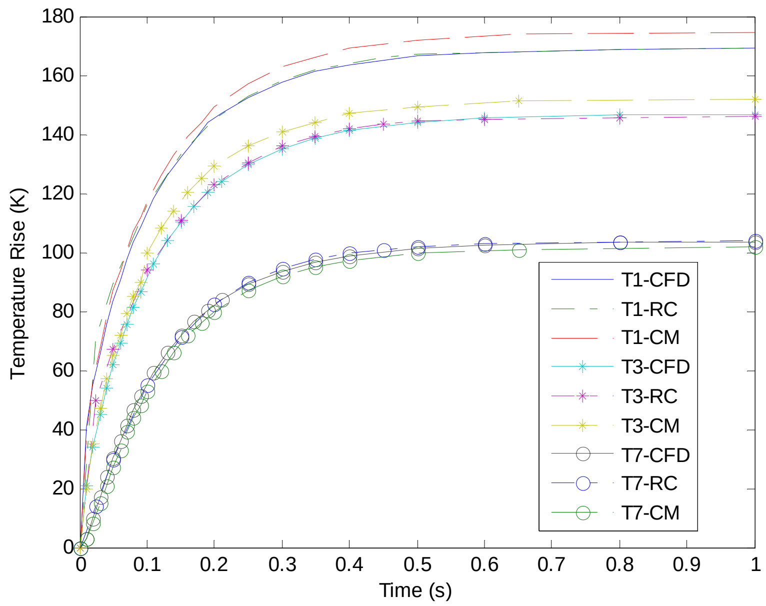



Figure 5.16 Temperature comparisons of three methods

The interface temperature rises at $T_1$, $T_3$, and $T_7$ obtained by multi-layer compact model (CM) are shown in Figure 5.16, with those by detailed modeling (CFD) and thermal resistance network modeling (RC) as well. It can be seen the results achieved by compact modeling are very close to that of detailed modeling with approximation error of 3.0%, while the mesh size has been reduced from 231,398 to 151,293, with a reduction of 34.6%. This shows the multi-layer compact is accurate and efficient and can be used for module level simulation.

### 5.4 Module Level Simulation

The detailed model for the IGBT module is shown in Figure 5.17, and the corresponding multi-layer compact model is shown in Figure 5.18. The temperature contours at $T_3$ and $T_7$ locations obtained by detailed modeling and multi-layer compact modeling under steady state are shown in Figure 5.19, indicating close agreement between the two. The thermal interaction between adjacent devices through the substrate and base plate is accurately captured by the compact modeling from Figure 5.19. It can also be seen that the thermal interaction between two devices in diagonal direction is so weak that it can be neglected. The approximation error under steady state is less than 3.5% for the case under investigation. The mesh size of the detailed CFD model is 505,433, while that of the compact model is only 368,786, with a reduction of 27.1%. The simulation time was down from 35 minutes to 23 minutes, reduced by 34.2%. Larger reduction for mesh size and run time is expected for a module with more devices. The comparison of transient simulations will be given later.

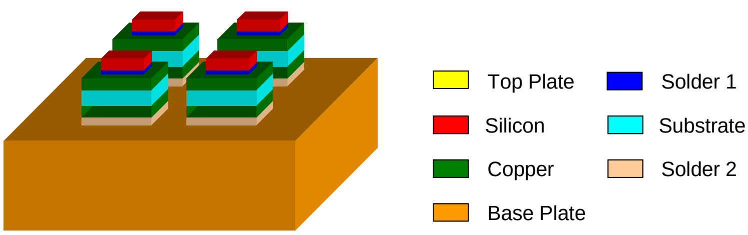



Figure 5.17 Detailed model of IGBT module

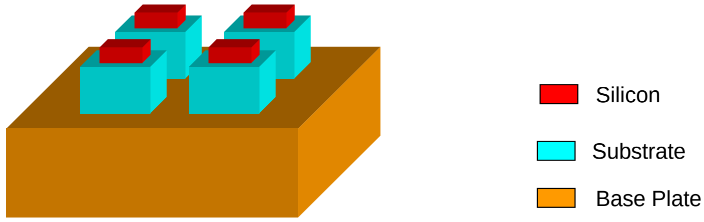
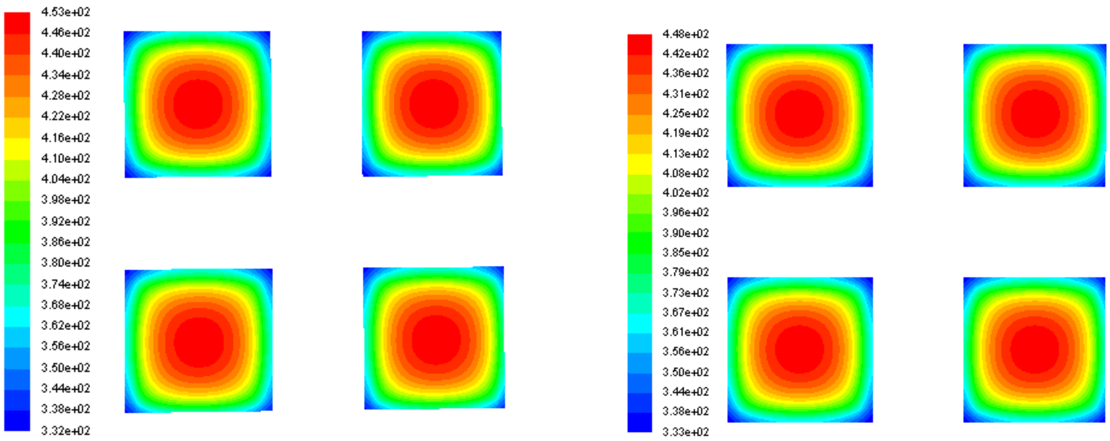
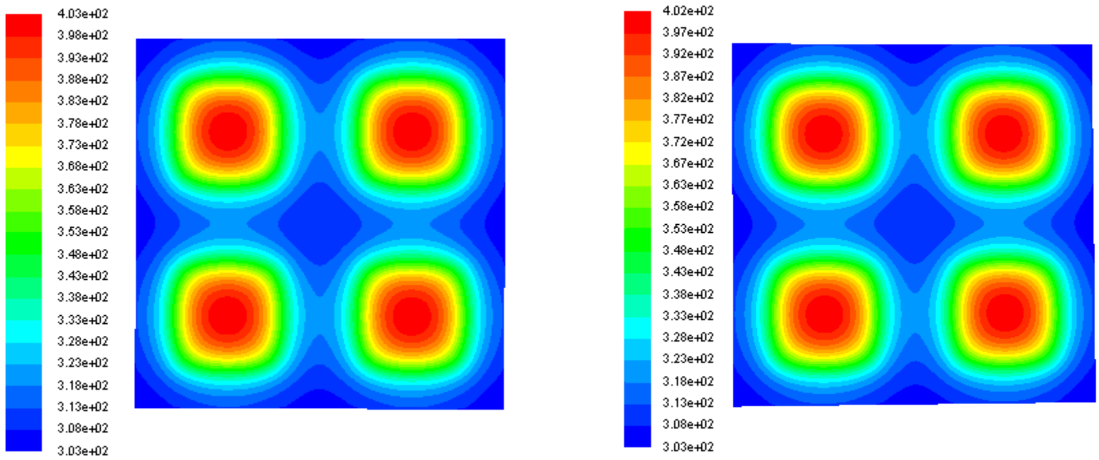



Figure 5.18 Multi-layer compact model of IGBT module




(a)




(b)

Compact modeling Detailed modeling

Figure 5.19 Temperature contours obtained by two methods at (a) $T_3$, (b) $T_7$

The thermal resistance network modeling can also be used to obtain the junction temperature. However, necessary modifications to the thermal resistance network shown in Figure 5.14 are needed to capture the thermal interaction between adjacent devices. A thermal resistor can be added between each pair of adjacent device to capture this effect. The value of the thermal resistor is calculated from the volume in the base plate shared by two adjacent devices. Thermal resistance network for the IGBT module is shown in Figure 5.20. $Q_i$ represents the heat source of the $i$th IGBT device, whose notation is shown in Figure 5.21. $T_{ij}$ represents the temperature at the $j$th interface of $i$th device.

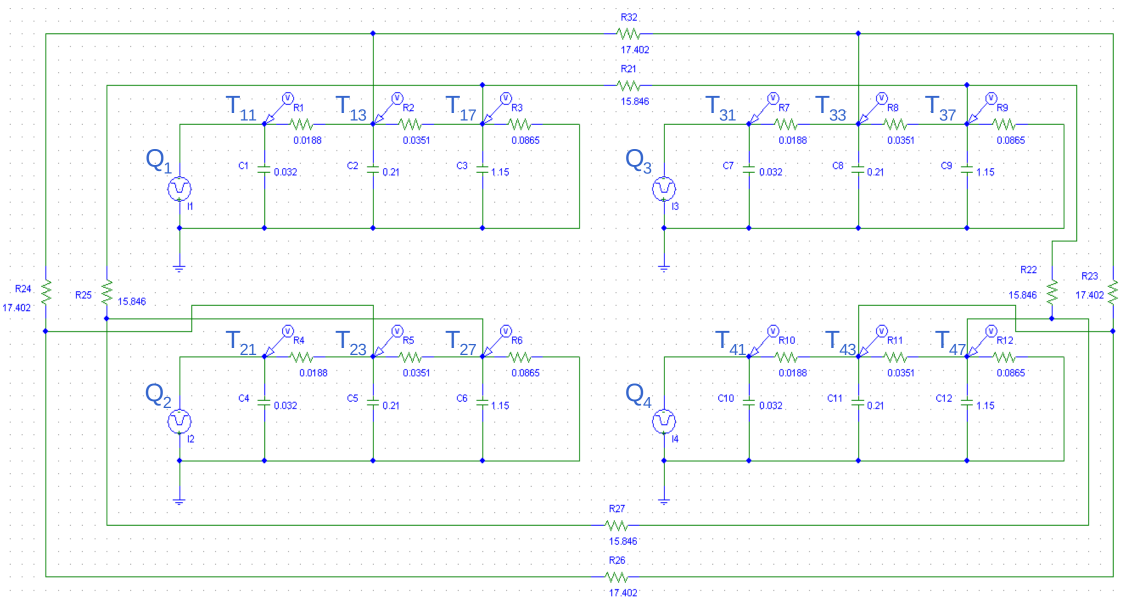



Figure 5.20 Thermal resistance network of IGBT module

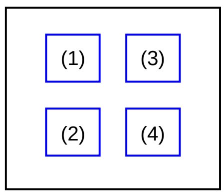



Figure 5.21 Notation of IGBT device

To compare the simulation results achieved by detailed CFD/HT simulation, compact modeling, and RC resistance modeling, steady state and transient simulations are conducted with these three methods. Four cases have been performed to compare the results of these methods under steady state, whose conditions are shown in Table 5.6.

Table 5.6 Simulation cases of three methods

| Case 1 | Case 2 | Case 3 | Case 4 | Method 1 | Method 2 | Method 3 |
|---|---|---|---|---|---|---|
| $Q_1$=1200W<br>$Q_{2,3,4}$=0W | $Q_{1,2}$=1200W<br>$Q_{3,4}$=0W | $Q_{1,2,3}$=1200W<br>$Q_4$=0W | $Q_{1,2}$=1200W<br>$Q_{3,4}$=1200W | CFD | Compact | RC |

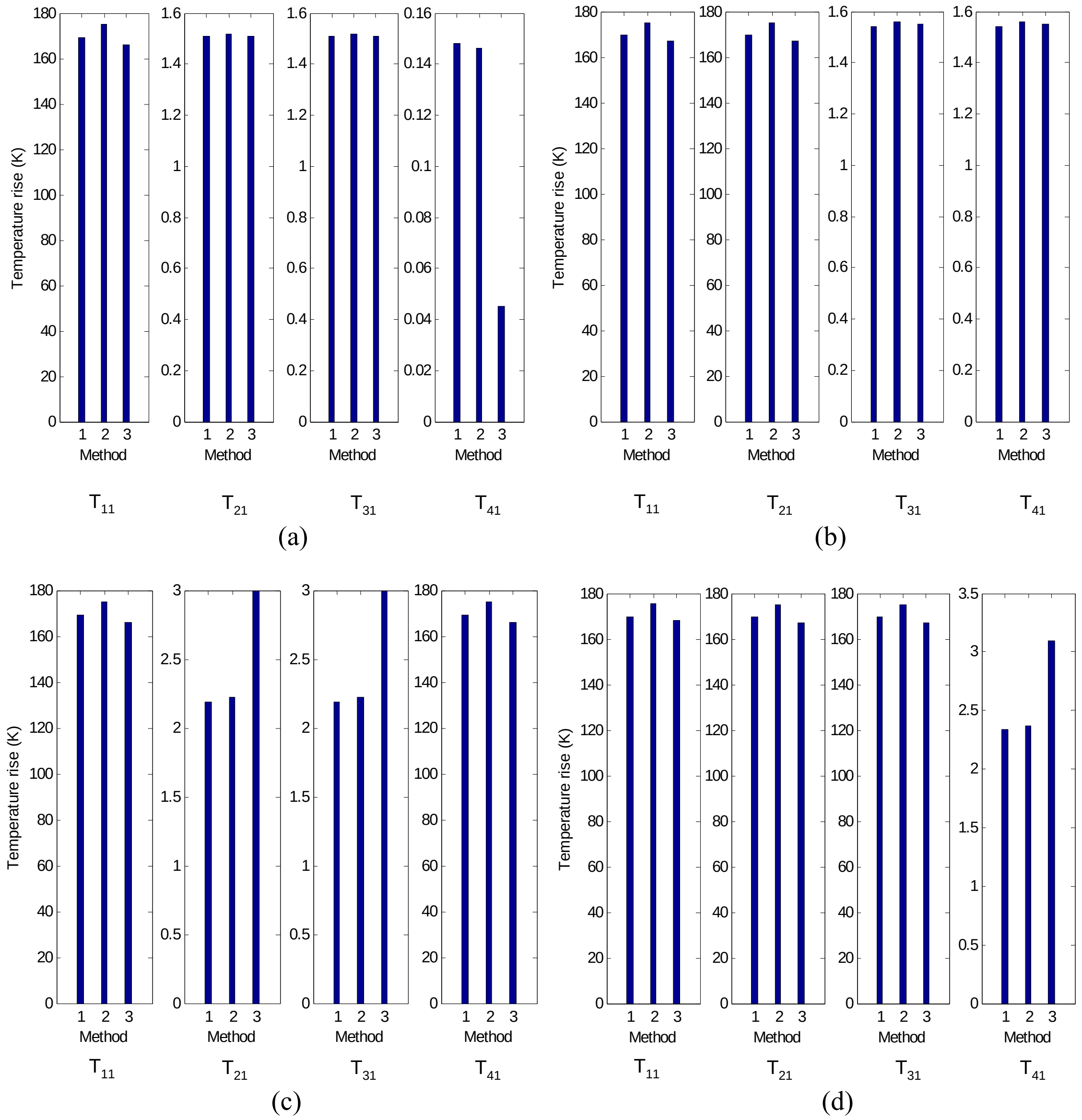



Figure 5.22 Temperature $T_{ij}$ obtained by three methods

The temperature $T_{ij}$ under four test cases are shown in Figure 5.22. It can be seen the results by four methods are very close to each other for the powered on IGBT devices.

The predictions of RC method are somewhat far away from those by the CFD/HT simulation and compact modeling for the device having the lowest temperature, with an error up to 300%. The compact modeling via multi-compact model predicted the temperature rise very well for all four cases, with a maximum approximation error of 6.0%, compared to the detailed CFD/HT simulations. Particularly accurate predictions have been achieved via compact modeling for IGBT devices suffering from maximum temperature.

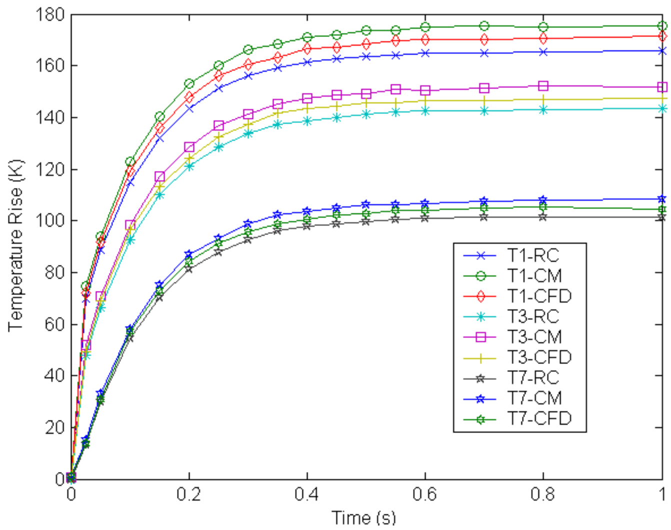


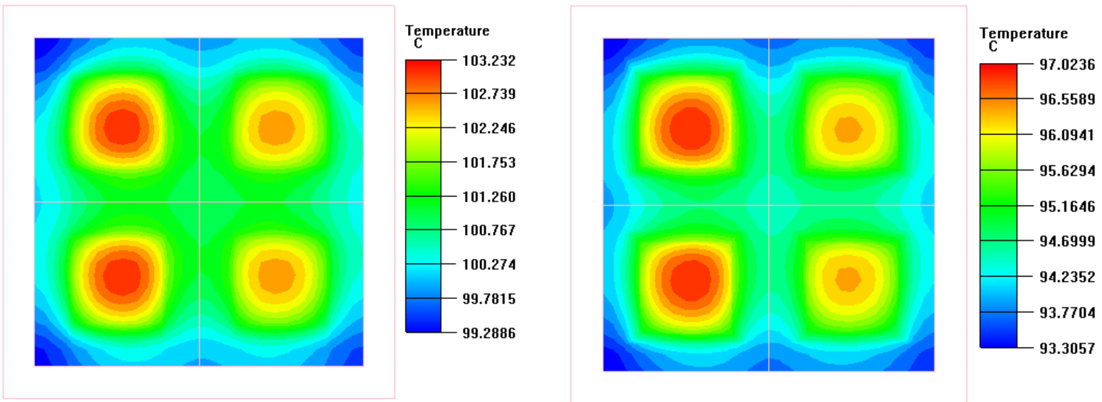

Figure 5.23 Temperature rise over time at $T_1$, $T_3$, and $T_7$

Figure 5.23 shows the temperature rise over time achieved by the detailed CFD/HT simulation, compact modeling (CM), and RC modeling for the Case 1 described in Table 5.6. The predicted trends of temperature variation by these three methods are very close to each other. The steady state temperature achieved by RC method is lower than the CFD/HT simulation, while that of CM is higher than CFD/HT. The approximation error of both CM and RC methods are less than 3.2% for the maximum temperature. This indicates that the compact modeling can be further used at system level simulation.

### 5.5 System Level Simulation

With successful simulation at component and module levels, the system level simulation for the system model shown in Figure 5.1 may be conducted. The heat sink is made of aluminum with 6 fins. The base and overall heights of the heat sink are 5 mm and 40 mm, respectively. The velocity of the ambient inlet air is assumed at 1 m/s. The outlet gauge pressure is assumed to be zero without losing generality. A heat source of 25 W is introduced for each IGBT device at the first row (upstream) and 20 W for each device at the second row (downstream). Three different approaches are investigated for the system level simulation as described below.

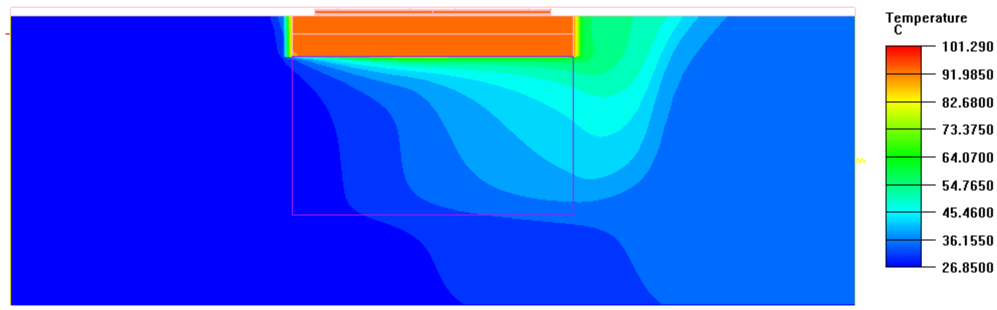
#### 5.5.1 Detailed CFD modeling and compact modeling



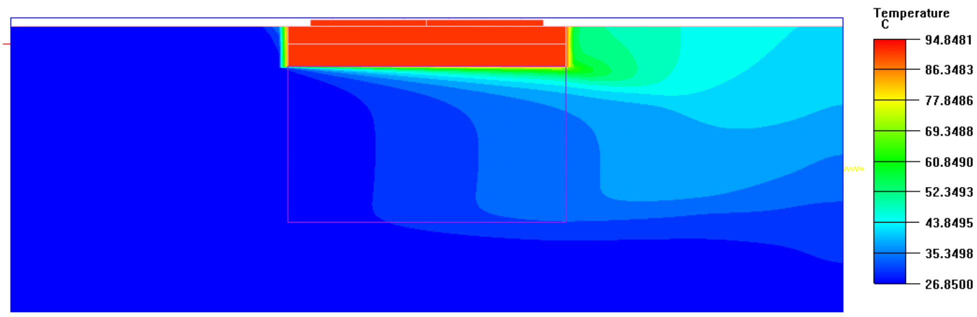

(a) (b)

Figure 5.24 $T_3$ contours, (a) CFD, (b) compact modeling

The system level simulation was conducted with two methods in this section. In the CFD/HT simulation, all components and therefore the module were modeled. Alternatively, compact models for the IGBT components and therefore the module can be included in the system level simulation, which is called compact modeling. Figure 5.24 shows $T_3$ of each device at steady state obtained by detailed CFD/HT simulation and compact modeling respectively. The temperature contours at z-middle plane (z=61mm) obtained by both methods are shown in Figure 5.25. The predicted temperature contour at $T_3$ by compact modeling is close to that of CFD/HT simulation with an approximation error less than 7.2%. The temperature contour at z-middle plane predicted by compact modeling has larger relative error (around 8.5%). The mesh size of the compact model is 998,731, compared to 1,426,887 for the detailed CFD model, a reduction of about 30.1%. In the meanwhile, the computation time has been reduced by about 26.7% from 4.5 hours down to 3.3 hours.




(a)




(b)

Figure 5.25 Temperature contour at z=61mm (a) CFD, (b) compact modeling

### 5.5.2 POD reduced order modeling

The POD reduced order modeling has been proved to be an efficient method with reasonable accuracy for the thermal/fluids analysis of complex systems, especially for the system level simulation. The application of POD reduced order modeling to the transient thermal analysis of the system model under investigation is described in this section. Two different POD approaches are illustrated through an example of enclosure.

**(1) Galerkin Projection based POD**

Extensive studies have been focus on the Galerkin Projection and its application to fluid control [46, 50, 93]. For the demonstration, consider a three-dimensional steady-state incompressible turbulent flow with negligible buoyancy effects, the transient Reynolds Averaged Navier-Stokes (RANS) continuity, momentum and energy equations are

$$\nabla \cdot \mathbf{u} = 0 \tag{5.9a}$$

$$\frac{\partial \mathbf{u}}{\partial \mathbf{t}} + \mathbf{u} \cdot \nabla \mathbf{u} - \nabla \cdot (\nu_{eff} \nabla \mathbf{u}) + \frac{1}{\rho} \nabla P = 0 \tag{5.9b}$$

$$\frac{\partial T}{\partial t} + \rho c_p \mathbf{u} \cdot \nabla T - \nabla \cdot (\kappa_{eff} \nabla T) = 0 \tag{5.9c}$$

Where $\nu_{eff} = \nu + c_\mu \dfrac{\kappa^2}{\varepsilon}$ and $\kappa_{eff} = \kappa + \dfrac{c_p \nu_t}{\rho \Pr_t}$, and can be computed through any RANS-based turbulence model and non-equilibrium wall functions [69]. Before we look at the Galerkin projection method, the centering was conducted to eliminate the velocity and temperature fluctuation:

$$\mathbf{u}(x,t) = \mathbf{u_o}(x) + \mathbf{v}(x,t) = \mathbf{u_o}(x) + \sum_{k=1}^{n} a_k(t) \varphi_{\mathbf{0}}(x) \tag{5.10}$$

$$T_f(x,t) = T_o(x) + T(x,t) = T_o(x) + \sum_{k=1}^{n} b_k(t) \phi_k(x) \tag{5.11}$$

where $\mathbf{u_o}(x)$ and $T_o$(x) are defined by

$$\mathbf{u_o}(x) = \frac{1}{n} \sum_{k=1}^{n} \mathbf{u}(x, t_k) \tag{5.12}$$

$$T_o(x) = \frac{1}{n}\sum_{k=1}^{n} T(x, t_k) \tag{5.13}$$

respectively. The idea of Galerkin Projection method is to project the governing equations to the POD spanned space. For the momentum equation, we have

$$(\boldsymbol{\varphi}_i, \frac{\partial \mathbf{u}}{\partial t} + (\mathbf{u}\cdot\nabla)\mathbf{u} + \frac{1}{\rho}\nabla P - \upsilon_{eff}\nabla^2\mathbf{u}) = 0 \tag{5.14}$$

A series of ODEs on the weight coefficients of velocity POD modes

$$\dot{a}_i + C_{ijk}a_j a_k - D_{ij}a_j + A_{ijk}a_j a_k + S_i + B_i = 0 \tag{5.15a}$$

Where

$$C_{ijk} \equiv \int_\Omega \boldsymbol{\varphi}_i \cdot (\boldsymbol{\varphi}_j \cdot \nabla)\boldsymbol{\varphi}_k dx \tag{5.15b}$$

$$D_{ij} \equiv \int_\Omega \boldsymbol{\varphi}_i \cdot \nabla^2 \boldsymbol{\varphi}_j dx \tag{5.15c}$$

$$A_{ijk} \equiv \int_\Omega \boldsymbol{\varphi}_i \cdot (\vec{u}_o \cdot \nabla\boldsymbol{\varphi}_j + \boldsymbol{\varphi}_k \cdot \nabla\vec{u}_o)dx \tag{5.15d}$$

$$S_i \equiv \int_\Omega \boldsymbol{\varphi}_i \cdot (\vec{u}_o \cdot \nabla\vec{u}_o - \nabla^2\vec{u}_o)dx \tag{5.15e}$$

$$B_i \equiv \int_\Omega \boldsymbol{\varphi}_i \cdot \nabla P dx = \int_\Omega \nabla\cdot(\boldsymbol{\varphi}_i P) - P(\nabla\cdot\boldsymbol{\varphi}_i)dx \tag{5.15f}$$

where summation over repeated indices is implied. The convective term $C_{ijk}$ results from the convective operator $\mathbf{u}\cdot\nabla\mathbf{u}$, the diffusive term $D_{ij}$ is from $\upsilon_{eff}\nabla^2\mathbf{u}$, the cross term $A_{ijk}$ is the cross operation between the source function and the POD modes, $S_i$ comes from the source term only and $B_i$ is the projection of the POD modes onto the pressure term, $\frac{1}{\rho}\nabla P$. The pressure on the boundary has physical significance because it provides the driving force for the flow. The main obstacle for inhomogeneous boundary conditions is the treatment of the boundary pressure and specifically coupling the pressure to the velocity field on the boundary in order to drive the flow. For homogeneous boundary conditions, $B_i = 0$ because $\int_{\partial\Omega} P\boldsymbol{\varphi}_i \cdot \mathbf{n}ds = 0$, and $\int_{\partial\Omega} P\boldsymbol{\varphi}_i \cdot \mathbf{n}ds = 0$ for periodic boundary conditions if there is no mean pressure gradient at the boundary. Therefore, the boundary term in (5.15a) is eliminated.

For the energy equation, using Galerkin Projection yields

$$(\phi_j, \frac{\partial T_f}{\partial t} + \mathbf{u} \cdot \nabla T_f - \alpha \nabla^2 T_f) = 0 \tag{5.16}$$

Similarly, a set of ODEs on the weight coefficients of the temperature POD modes can be obtained

$$\begin{aligned} \frac{db_j}{dt} &= -(\phi_j(x), \bar{u}(x) \cdot \nabla T_o(x)) - (\varphi_j(x), U(x) \cdot \sum_{k=1}^{n} \nabla \varphi_k(x) b_k(t) \cdot \nabla T_o(x)) \\ &\quad - (\varphi_j(x), \sum_{k,j=1}^{n} \phi_k(x) a_k(t) \cdot \nabla(\varphi_k(x) b_k(t)) - \alpha(\varphi_j(x), \nabla T_o(x))) \\ &\quad - \alpha(\sum_{k=1}^{n} b_k(t)(\nabla \varphi_j(x), \nabla \varphi_k(x)), j = 1, 2, ..., n \end{aligned} \tag{5.17}$$

Given necessary boundary conditions, the Equations (5.15) and (5.17) can be solved numerically, e.g. with fourth order Runger-Kutta method.

**(2) Coefficients interpolation**

As noted above, the Gelerkin Projection is difficult to solve for inhomogeneous boundary conditions. A simplified approximation method to get the weight coefficients is proposed in [83]. The weight coefficient of each POD mode for any snapshot can be obtained with following inner product

$$\{(\mathbf{u}(x,t) - \bar{\mathbf{u}}(x)) \cdot \sum_{k=1}^{n} a_k(t) \boldsymbol{\varphi}_k(x)\} = 0 \tag{5.18}$$

$$\{(T_f(x,t) - T_o(x)) \cdot \sum_{k=1}^{n} b_k(t) \phi_k(x)\} = 0 \tag{5.19}$$

For any time $t = \tau$, the new weight coefficients $a_k(\tau)$ and $b_k(\tau)$ can be obtained by interpolating the weight coefficients $a_k(t)$ and $b_k(t)$ ($t$=0, $t$).

**(3) Illustration of two methods**

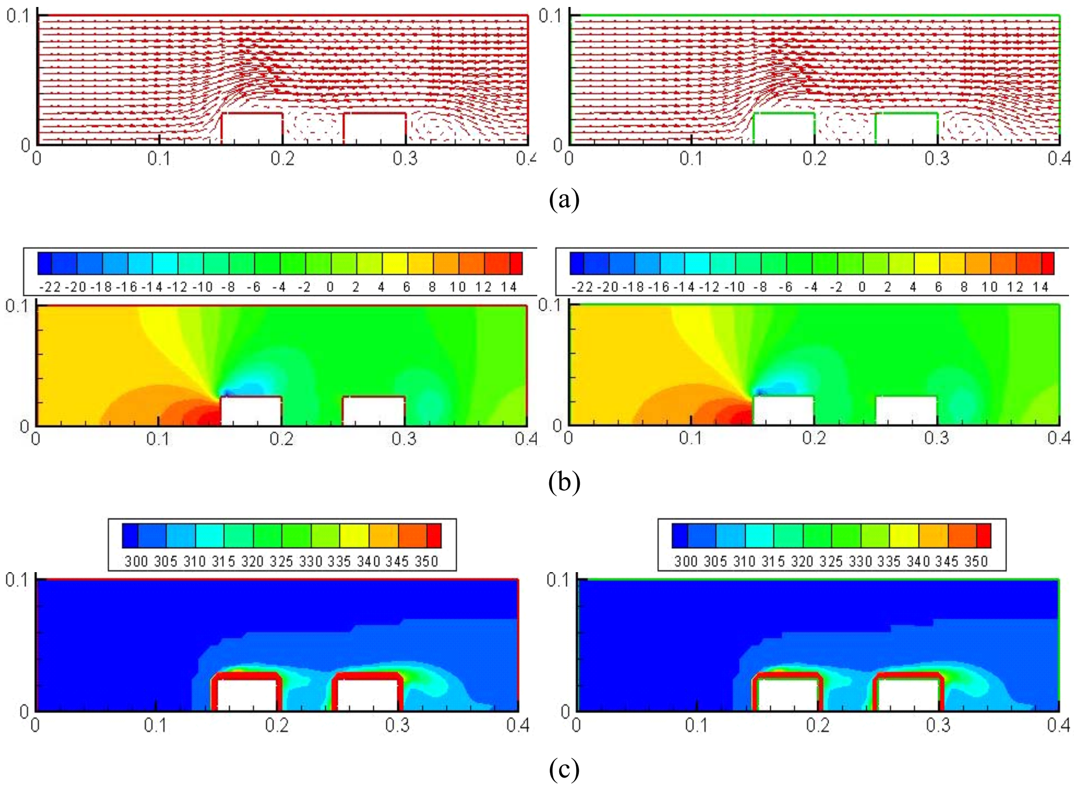


Figure 5.26 Results via CFD/HT (left) and Gelerkin Projection (right), (a) velocity, (b) pressure, (c) temperature

To demonstrate the two methods above, consider the server model shown in Figure 6(b). Assume the initial conditions are $V_{in}$=2 m/s, $T_{in}$=300 K, $T_c$=350 K. At t > 0, the boundary conditions are changed to $V_{in}$=4 m/s, $T_c$=500 K. The simulation results at t=0.0224s predicted by CFD/HT and Galerkin-Projection POD are shown in Figure 5.26. A maximum error of less than 5% is achieved for POD based modeling with Galerkin Projection method. Figure 5.27 depicts the results by the coefficients interpolation POD reduced order modeling and the CFD/HT simulation as well. It can be seen that the results through coefficients interpolation are also close to the CFD/HT simulations, with an approximation error of 7.1% for the current test case. The reason that interpolation yields acceptable results is that only one-dimensional interpolation is needed in time domain.

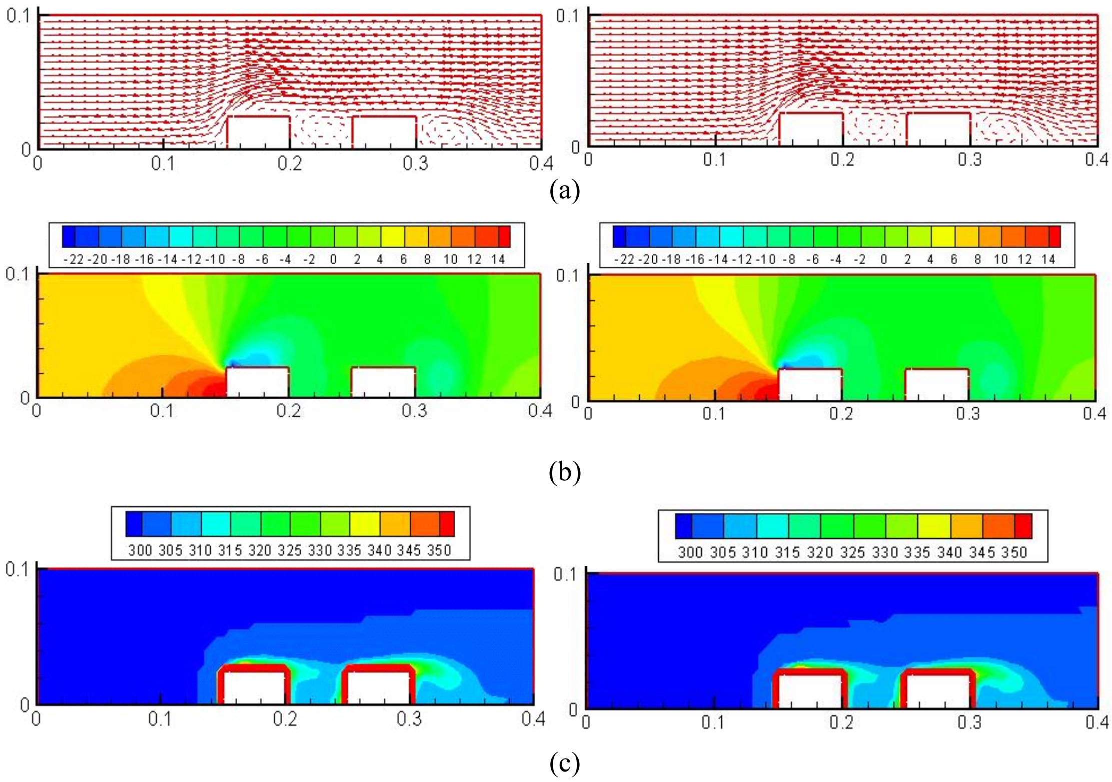
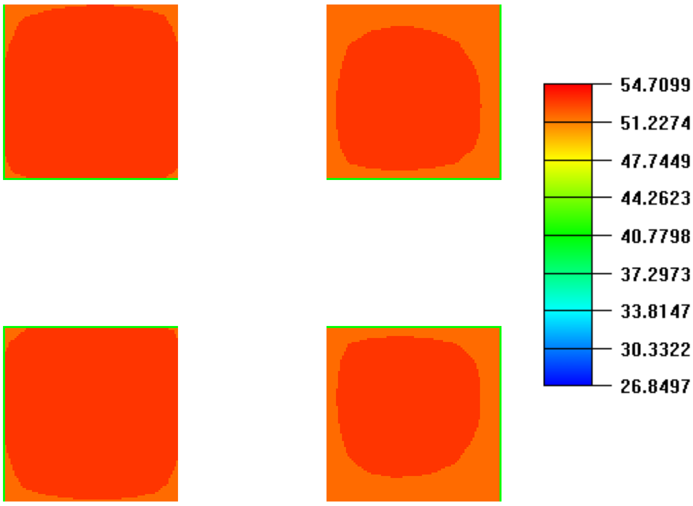


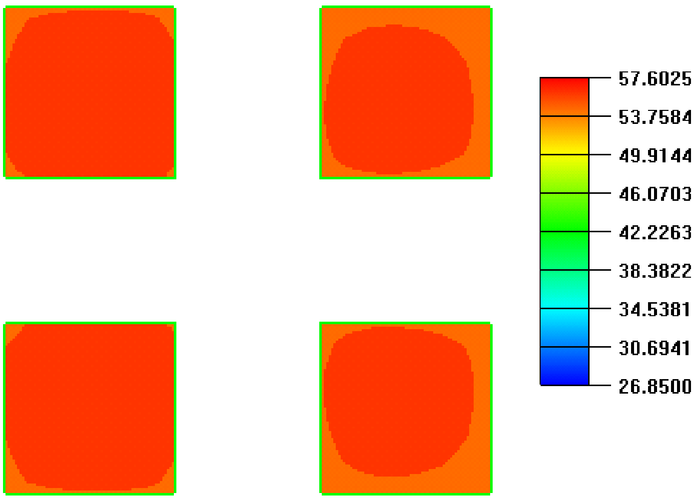

Figure 5.27 Results via Galerkin projection (left) and interpolation (right), (a) velocity, (b) pressure, (c) temperature

**(4) Application of coefficients interpolation based POD**

As noted above, the interpolation based POD method works well for transient scenario, without dealing with the complex inhomogeneous boundary conditions. It was used to solve the model problem shown in Figure 5.1. A time step of 1 s and 400 steps are used for the transient simulation. The snapshots are generated every 20 s, yielding a total of 20 snapshots. Figure 5.28 shows the temperature and velocity fields at the z-middle plane at t=70 s obtained by both CFD/HT simulation and interpolation based POD methods. An approximation error of 7.1% for the velocity and 9.8% for the temperature fields is achieved by the POD method, while the run time has been reduced from 7.5 hours to 2.5 minutes by using POD based reduced order modeling.




(a)




(b)

Figure 5.28 Temperature contour of $T_1$ at t=70 s, (a) CFD/HT, (b) POD

# CHAPTER 6

# EXPERIMENTAL SETUP AND MEASUREMENTS

High power density packaging of power semiconductor devices presents some of the greatest thermal design challenges due to the resulting high heat fluxes. Advanced cooling techniques involving double-sided cooling can help to meet these demands for current and future semiconductor devices [94-96]. These advanced cooling techniques can improve power density greatly if they can be interfaced properly with the semiconductor device packaging technology. To demonstrate that the developed reduced order modeling methodology from previous chapters can be also applied for electronic systems utilizing such advanced cooling techniques, a test vehicle with hybrid cooling technique is built and fully tested in this chapter.

## 6.1 Double-Sided Cooling

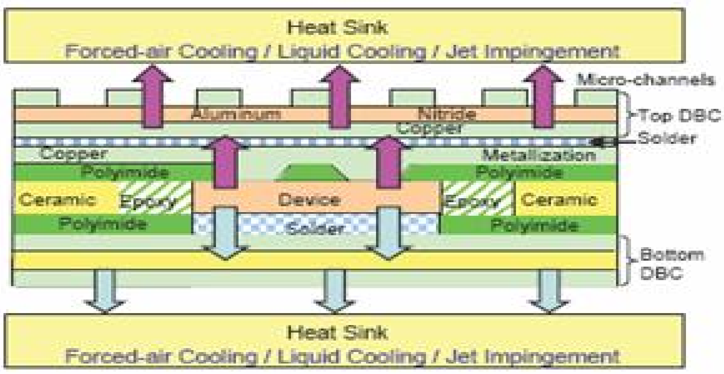



Figure 6.1 Double-sided cooling of power electronic module [96]

The idea of double sided cooling was originally proposed by Gillot [96] for power electronic modules, as shown in Figure 6.1. All components of the module are connected in parallel and are sandwiched between two direct bond cooper (DBC) substrates.

Cooling devices can be attached to both sides of the module so that heat can be dissipated through both sides. This concept has been increasingly studied by simulation and experimental work at device level [97, 98]. In this work, this concept is first studied at the system level.

### 6.2 Test Vehicle with Hybrid Cooling

Figure 6.2 Physical test vehicle

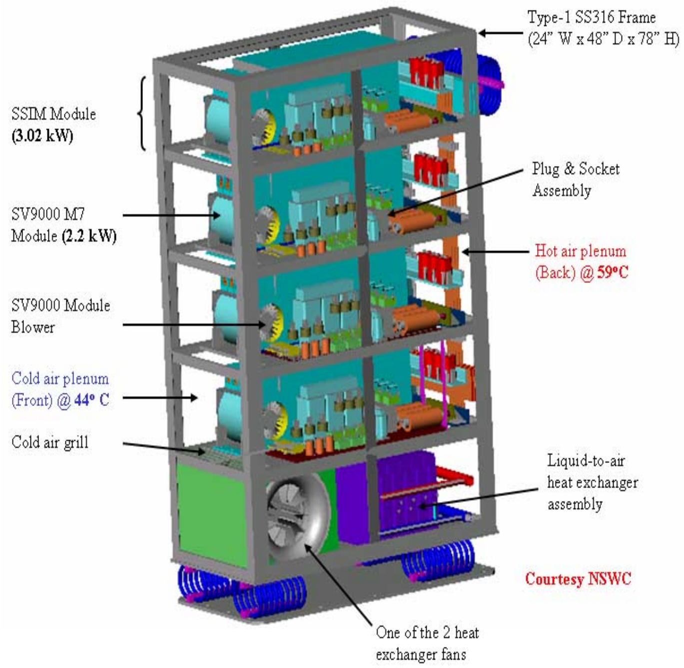



Figure 6.3 PCM-1 cabinet

A test vehicle with hybrid and double-sided cooling is constructed, as shown in Figure 6.2. Its configuration is based on a prototype power conversion module (PCM) cabinet called PCM-1 [99], as shown in Figure 6.3. PCM-1 cabinets are used to distribute power in various ship zones. This test cabinet consists of four enclosures and one bottom bay, with each enclosure containing three packages, as shown in Figure 6.4(b). The air is contained inside the cabinet and circulated by the blower and fans, as depicted in Figure 6.4(a). The detailed configuration of the package is illustrated in

Figure 6.4(c). A thermoelectric module (TEC) with heat sink is attached to the top of the package to provide a heat flow path from the top. To achieve cooling from the bottom of the package, a microchannel cooler is directly attached to the substrate of the package. It is noted that wire-bonding technology, instead of the traditional flip chip technology was utilized, so that the substrate and the microchannel cooler can be contacted directly to reduce the contact thermal resistance, without introducing design complexity and electrical isolation issues. An aluminum nitride substrate is also used in this configuration to enhance the cooling from the bottom of the package. With this configuration, a double-sided and hybrid forced air convection, thermoelectric cooling, and microchannel cooling approach is achieved.

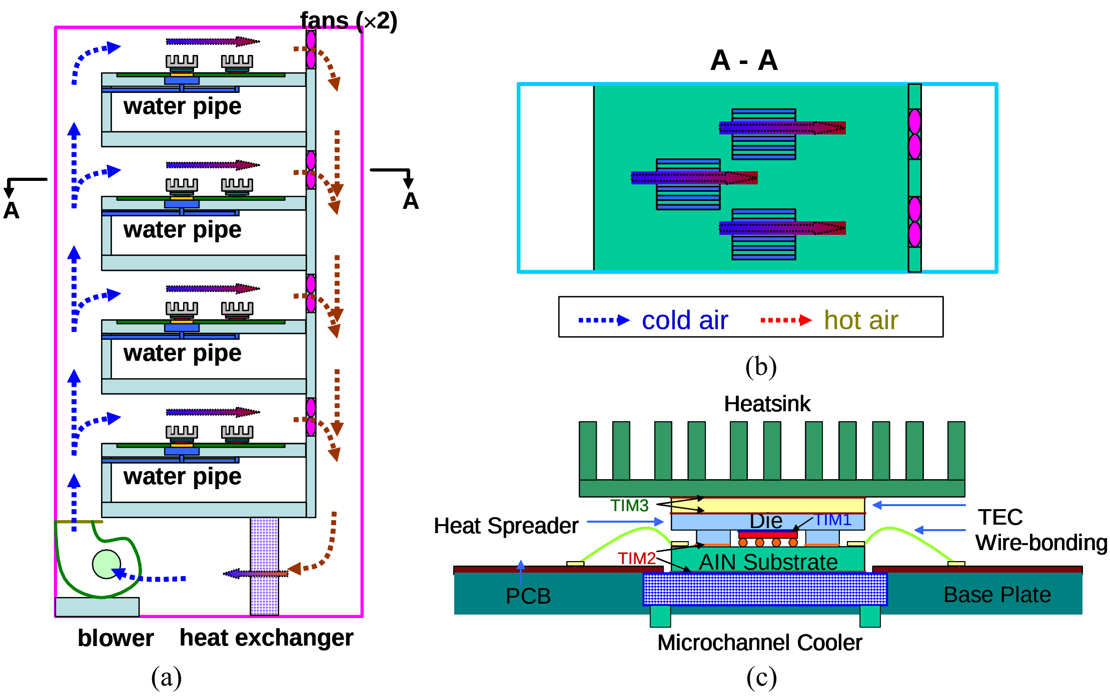



Figure 6.4 Schematic of (a) system, (b) enclosure, and (c) package

### 6.3 Experimental Setup for Thermal Management Study of Cabinet

A schematic of the experimental setup is shown in Figure 6.5. A temperature control unit (TCU) (Sterling Micro Series 460230) stabilizes the temperature of the chilled water to be within ± 0.56 °C (± 1 °F) from the chiller and drives the chill water through flow maters to the heat exchanger and test chips. The chilled water picks up the heat from the microchannel cooler at each package and the heat exchanger at the bottom bay and goes back to the chiller through TCU, whose schematic is shown in Figure 6.6. Part of the hot water coming out of the test vehicle will return to the chiller through the TCU, and the rest will be recirculated within the TCU through the circulating pump inside the TCU. The immersion heater inside the TCU will be automatically switched on and heat the water if the recirculating water temperature is below the set point. A bypass loop is used to adjust the flow rate and pressure to the test vehicle. The cool sensor and heat sensor are used to monitor the return water temperature and supply water temperature so that the immersion heater can be switched on and off through the PID fuzzy control logic. The system safety is maintained through a safety thermometer and pressure relief valve. The maximum operating temperature and pressure of the TCU is designed to be 121 °C (250 °F) and 1,034,214 Pa (150 PSI), respectively. Two pressure gauges are used to monitor the water pressure at the inlet and outlet of the test vehicle, respectively. Another two pressure gauges are used to monitor the pressure drop across the microchannel cooler attached to the left chip package in the third enclosure from the below. The water flow rate through each microchannel cooler of the package is adjusted by a flow meter. Eight DC power supplies are used to power the chips and TEC modules, and the temperature signals are collected through a data acquisition system and processed through a PC.

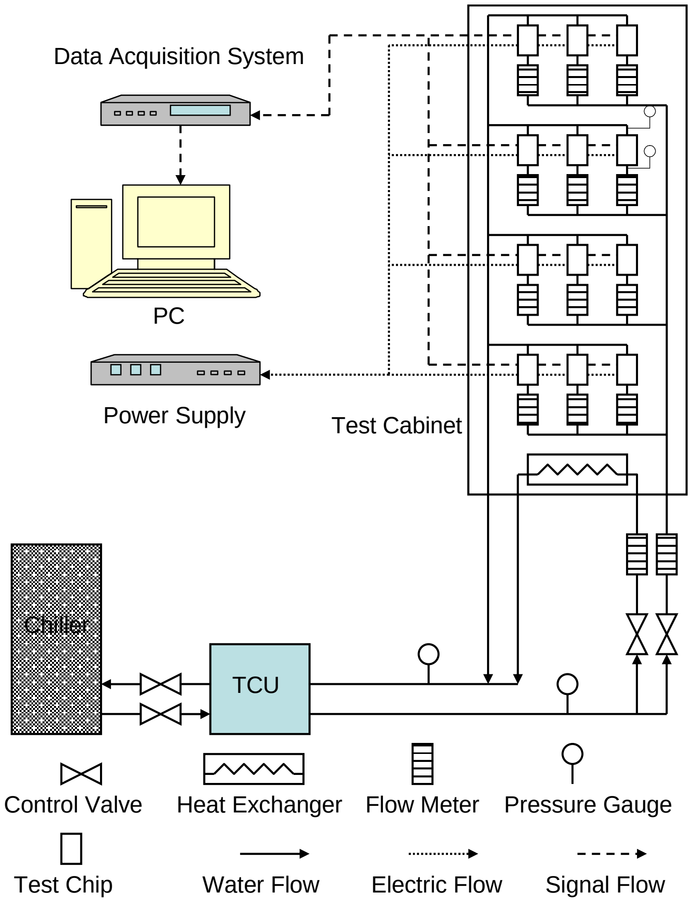



Figure 6.5 Schematic of test flow loop

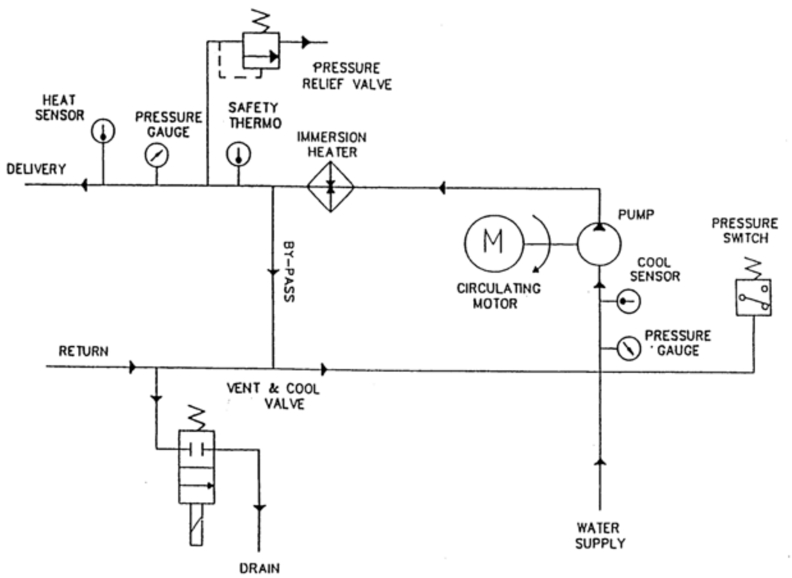



Figure 6.6 Flow diagram of the TCU

### 6.3.1 Thermal Test Module

A thermal test die (Delphi PST4-02) was used in the test vehicle to characterize the thermal performance of the package, whose layout is shown in Figure 6.7. Resistive heating in this thermal test die is accomplished by driving a current through a doped silicon well between a pair of bus bars, labeled $R_s$ and $R_f$. The 4 $R$ labeled pads accommodate Kelvin connections, if desired. At the top and bottom of the die are a pair of pads, labeled $D$ in the diagram, which connect a serial five-diode temperature sensor network. Again, a four-pad layout allows Kelvin connections, if desired. A second temperature monitoring circuit uses a bridge network by connecting the "V" at the top of the die and the "G" at the bottom of the die with one sense pin "S" at the top of the die and the other sense pin "S" at the bottom of the die. The five-diode string from the center is duplicated in all four corners. The corner diode strings are connected in series such that each corner can be monitored individually while driven by a single current source.

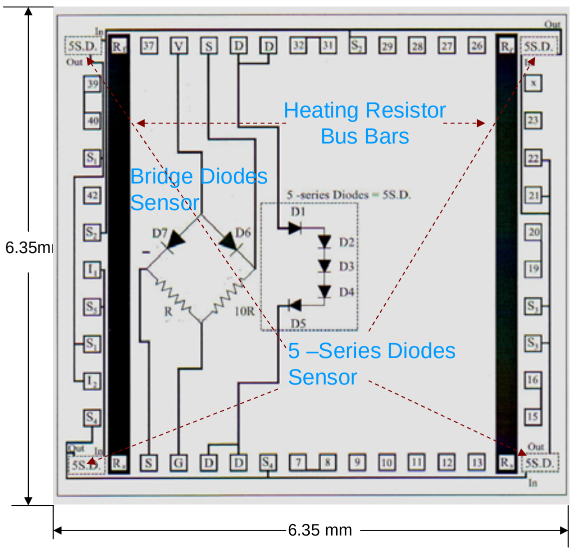



Figure 6.7 Layout of thermal test die

The thermal test die comes with 63Sn/37Pb solder with a UBM diameter of 178 microns, and a bump height of 140 microns, respectively. The thickness of the die, metal layer, and passivation layer are around 650 μm, 17,000 Å, and 10,000 Å, respectively. The metal composition is Al/Cu/Si (98/1/1). The pad information and detailed layout are listed in Appendix E.

Aluminum nitride (AlN) substrate is used to attach the thermal die, due to its much higher thermal conductivity (~170 W/K-m) than FR-4 substrate. The layout of the substrate is shown in Figure 6.8 (a). The non-solder mask defined (NSMD) printed circuit board (PCB) layout is utilized, as illustrated in Figure 6.8(b), due to its more closely controlled size and better copper adhesion to the laminate. The metallization of the pad is Pd/Ag (1/10), considering its low cost.

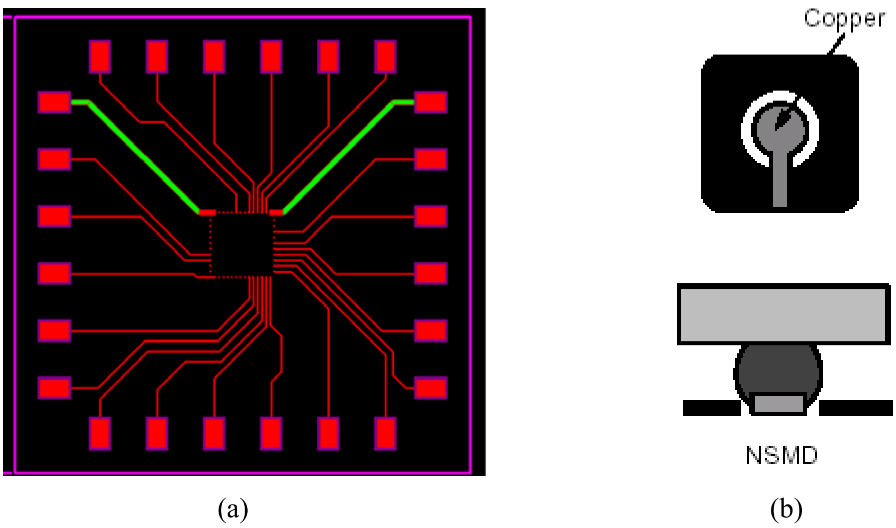


Figure 6.8 (a) Layout of AlN substrate (b) solder mask layout

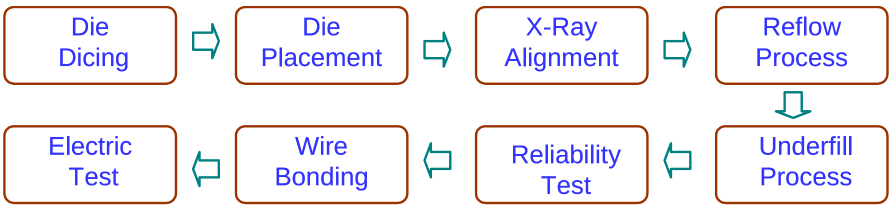


Figure 6.9 Package assembly procedure

The complete package assembly procedure is shown in Figure 6.9. It is noted that underfill materials are still necessary to reduce the coefficient of thermal expansion (CTE) mismatch between the substrate and silicon die, even though the CTE (~4.6) of aluminum nitride substrate is close to that of silicon (~3).

The layout of PCB is shown in Figure 6.10. FR-4 was used, since no major heat spreading is expected in the PCB. A hole is made at each package location, so that the micro-cooler can be attached to the AlN substrate directly. 12 six pins edge connectors are soldered to the PCB board for the power input and signal output.

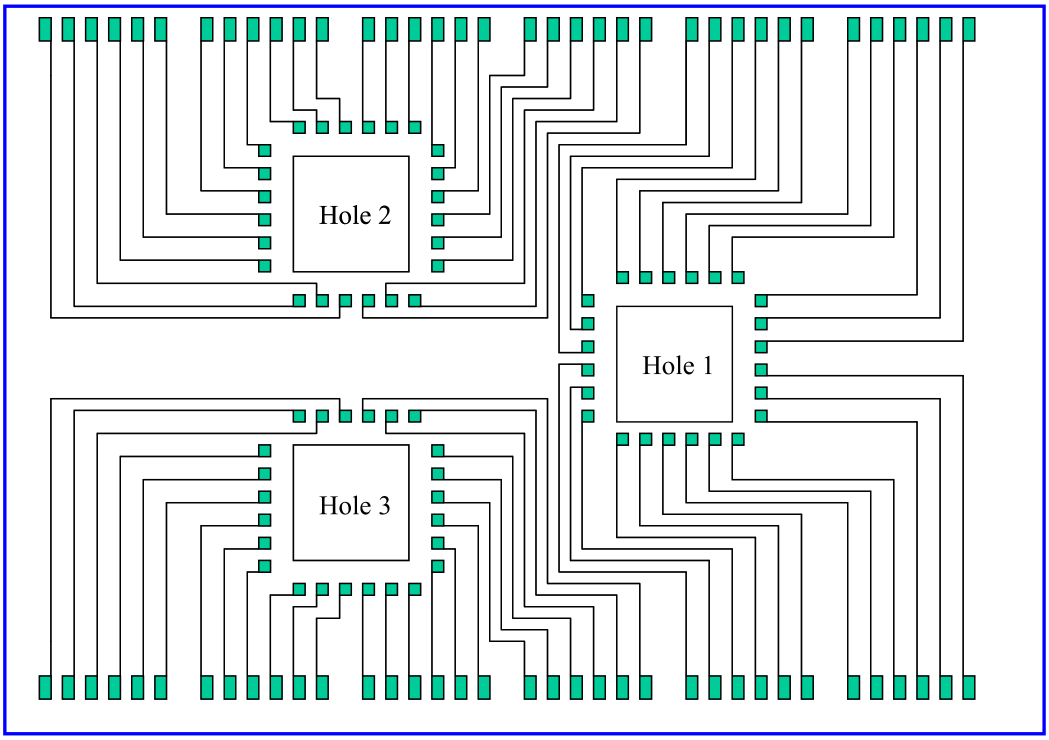



Figure 6.10 Layout of PCB

### 6.3.2 Thermal Test Die Theory and Measurement Facilities

The die temperature is monitored by the temperature-sensing diodes of the thermal test die. The schematic of temperature diode is shown in Figure 6.11. A strong voltage and temperature dependence exists in diode. The forward current $I_D$ through a diode can be characterized by

$$I_D = I_s\left(e^{\frac{q_e V_D}{k_B T}} - 1\right) \tag{6.1}$$

Where $I_s$ is the reverse saturation current, $k_B$ = 1.38×10$^{-23}$ J/K, and $q_e$ = 1.6 ×10$^{-19}$ Coulombs. Therefore, the forward voltage $V_D$ can be expressed as a function of temperature $T$

$$V_D = \frac{k_B}{q_e}\ln\left(\frac{I_D}{I_s}+1\right)T \tag{6.2}$$

Because it is relatively easy to measure the forward voltage and forward current, temperature $T$ can be easily calculated.

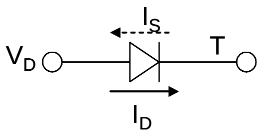



Figure 6.11 Schematic of temperature diode

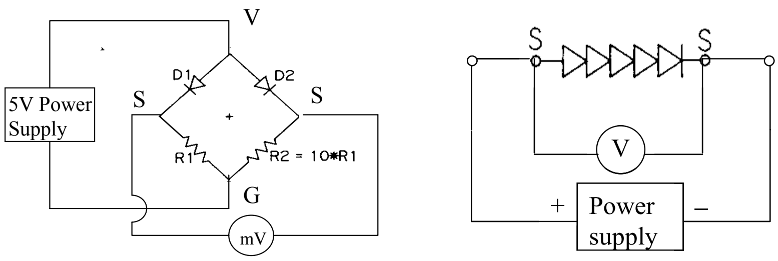



Figure 6.12 (a) Bridge temperature diodes (b) 5-series temperature diodes

There are two different configurations of the temperature diode in the thermal test die: bridge diodes and series diodes, whose schematics are shown in Figure 6.12 (a) and (b), respectively. For the bridge temperature diodes, the circuit is manufactured which will have two diodes at the same temperature but on conducting ten times the forward current of the other. A bridge configuration containing two diodes and two resistors will produce this set of conditions so long as the resistors are fabricated in a 10:1 ratio. The diode equation (6.2) still applies to both diodes. By simultaneous solution of Eq. (6.2) for the difference in forward voltage ($\Delta$ V) where the current in one circuit is ten times ($10I_D$ ) that of the other, the thermal response is

$$\frac{\Delta V}{\Delta T} = 0.2 \frac{mV}{^{\circ}C} \tag{6.3}$$

A DC power supply with an output voltage of 5 V was used to power the bridge diodes, and a voltmeter was used to monitor the voltage difference between two diodes. The readings should be within 56 mV and 62 mV at room temperature as per the manufacturer. The bridge diode configuration can provide effective noise rejection and avoid a constant current source. However, a very sensitive test equipment is needed, since a temperature variance of 1 °C will result in a variance of only 0.2 mV. For the series configuration, 5 diodes are connected in series and powered by a constant current (100 mA) power supply. The voltage drop across the 5 diodes was monitored by a voltmeter. Since the temperature response across one diode is 2 mV/°C, a total of 10 mV/°C will be expected for the temperature variance of 1 °C with the 5-series diodes. Compared to bridge diodes, 5-series diodes configuration does not require sensitive test equipment but needs a constant current source.

Six DC power supplies with dual outputs ranging from 0-30 V and 0-10 A were used to provide the heating to the chips, and one DC power supply with a range of 0-50 V and 0-16 A is used to power the TEC modules. A Lytron (CP-6310) air-liquid heat exchanger was used to cool the hot air from the enclosures. The inlet water temperature of the system is maintained at 10 ± 0.56 °C by the TCU during the experiment, and can be adjusted based on application. The ¾ HP centrifugal pump inside the TCU can supply a flow rate up to 56.78 l/min (15gpm).

For flow rate measurement, one flow meter with range of 1.893 to 9.464 l/min (0.5 to 2.5 gpm) was used to monitor the flow rate across the air-to-liquid heat exchanger, and 12 flow meters with range of 315.45 to 3,785.4 ml/min (5 to 60 gph) were used to measure the flow rate across each micro-cooler. The gauge pressures across each micro-cooler and the entire system are measured by multi-purpose dual scale pressure gauges. The inlet and outlet water temperatures of the air-to-liquid heat exchanger and micro-coolers were measured using J-type thermocouples with a sheath diameter of 1.57mm (0.062"), and the inlet and out temperatures of the air across the enclosure and heat exchanger are measured with T-type thermocouples (0.511 mm or 0.02"). The actual power input to the chip was determined by measuring the current and the voltage through and across the heaters, respectively. The temperature, resistance, current and voltage signals were collected using an Agilent 34970a data acquisition unit with two 34901A Multiplexers. The data were eventually transferred to a PC through a GPIB interface card.

### 6.4 Test Matrix and Measurement Calibration

A list of variables during experiments is shown in Table 6.1. Three different flow rates through the heat exchanger were tested to consider the effect of the flow rate on the thermal performance, e.g. chip junction temperatures. Also three different flow rates through each micro-cooler were considered. Experiments were also conducted to study the effect of the TEC on the chip junction temperatures. Measurements were conducted for the cases when the TEC modules are switched on and off. Also three different electric currents to the TEC modules were tested to investigate the temperature reduction achievable. The measurement results with different cooling methods (single-sided forced air convection (SAC), single-sided water cooling (SWC), double-sided cooling (DSC) and the corresponding cases with TEC) are compared.

Table 6.1 Testing matrix

| Parameters | Value |
|---|---|
| Flow rate through heat exchanger | 3.028 l/min (0.8 gpm), 5.678 l/min (1.5 gpm), 9.464 l/min (2.5 gpm) |
| Flow rate through micro-cooler | 314.45 ml/min (5 gph), 943.35 ml/min (15 gph), 3,785.4 ml/min (35 gph) |
| TEC current | 0.3 A, 0.8 A, 2.0 A |
| Cooling method | SAC, SWC, DSC<br>SAC with TEC, DSC with TEC |

The designed electric resistance of the heating circuit inside the thermal test die is 20Ω. But calibration is necessary, since this value may be different for different test die. Also, the values may change with the time. The external resistances such as those associated with solder connection and wiring may be different for each package. A pair of resistances for each package needs to be characterized, so that the right voltage or current can be selected in DC power supplies to these packages. Calibration of temperature diodes and thermocouples are also necessary for accurate measurements. Appendix B shows the electric resistances of each package and the calibration of temperature diodes and thermocouples.

It should be noted that 2-point method was used to measure the resistance of the heat resistor of the thermal test die. The four-pad configuration of the resistor allows 4-point measurement, which is expected to be more accurate than 2-point measurement when measuring small resistance in the milli- or micro-ohm range. The 4-point measurement may need to be considered when the length of the wires between the device and multimeter, due to the non-negligible resistance associated with the wires [100]. Since the resistance of each thermal test die is around 20 ohms and was measured separately right at the die location, the improvement of accuracy by 4-point measurements may be negligible.

The air temperature measurement points and chip indexes are shown in Figure 6.13. There are two thermocouples at the front of the heat exchanger (about 10 mm away from the front surface of the heat exchanger) to measure the inlet temperature of the air across the heat exchanger. Similarly, two thermocouples are put at the back of the heat exchanger to measure the backside air temperature. The averaged values of the readings from each pair of thermocouples are taken as the measurement values. Similarly, the averaged values of the measurements of the two thermocouples at the outlet of each enclosure are taken as the outlet air temperatures of the enclosure.

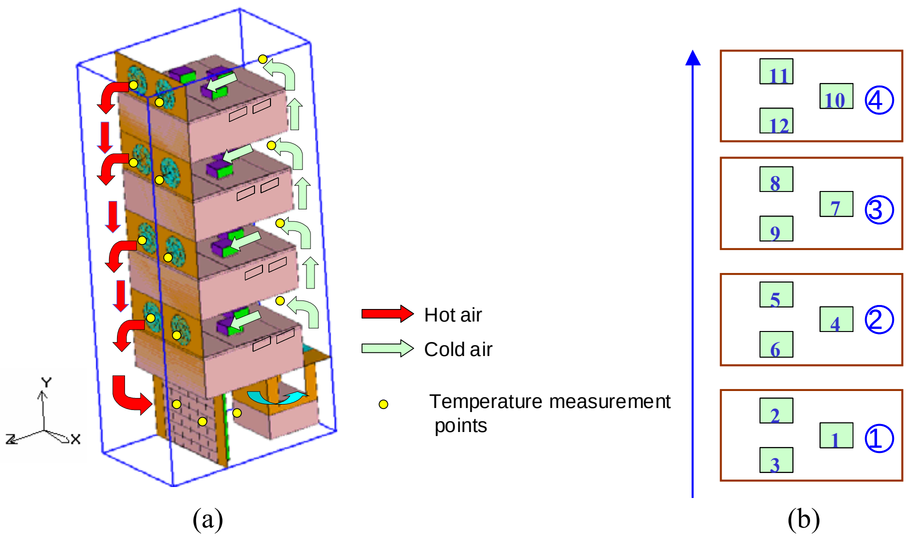



Figure 6.13 Temperature measurement points (a) air, (b) chip

## 6.5 Uncertainty Analysis

The inlet and outlet water temperature were measured using J-type thermocouples (with a sheath diameter of 1.57 mm or 0.062”). The thermocouples and the data acquisition system were collectively calibrated against a precision mercury thermometer at ice point to an uncertainty of ±0.4 $^{o}$C. Each set of temperature diodes was calibrated with two methods. The first method is to calibrate the readings of diodes against a calibrated thermocouple attached to the chip surface in a convective oven. Another method is against the readings of the oven temperature sensor. Resistance values of these diodes were recorded for each temperature setting. Very good linearity was observed, as shown in Appendix C.

Error sources for the temperature measurement include the calibration uncertainty due to the thermocouple and uncertainties due to curve fitting. The latter is estimated to be within ±0.2 $^{o}$C. Combining these effects gives an uncertainty of ±0.21 $^{o}$C. The uncertainty of T-type air temperature measurement is estimated to be within ±0.25 $^{o}$C from manufacturer data and curve fitting. A slightly higher uncertainty of K-type thermocouple measurement is estimated, which is within ±0.5 $^{o}$C. The power dissipation is determined from the product of the voltage and current measured at the heating circuit inside the thermal test dies. In this experiment, a constant current is provided for each thermal test die, and the readings (products of the voltages and currents) from DC power supplies are taken as the measurements of power dissipations of test dies. Constant current source is better than constant voltage source in this case, due to voltage drop across external wires and solders. By measuring the voltage across the thermal test die, the power to the thermal test die can be obtained. The current measurement has ±0.2 % uncertainty, as indicated by the product manual. For the voltage measurement, an uncertainty of ±0.3% results for the 30 V case. These uncertainties cause a ±0.5% uncertainty in power input measurement. It was found that the power input measurement agreed within 5% with the heat transferred to water. The inlet chilled water temperature oscillates within ±0.56 °C. Combining the uncertainties in temperature diodes and heat dissipation and chill water temperatures gives the uncertainties of total temperature measurement of chip at around 2%, and temperature measurement of air and water at around 8%.

As for flow rate measurement, an uncertainty of ±4 % is estimated for the flow rate through micro-cooler as indicated by the product manual. The water flow rate through the heat exchanger has an uncertainty of ±3 % as indicated by the product manual. The pressure measurement uncertainty is estimated at ±2 % from the product manual.

### 6.6 Experimental Study

Experiments were conducted to evaluate the thermal performance of test vehicle with hybrid cooling using the approaches described above. Forced air convection cooling only, double-sided cooling, and water cooling only were tested for chip load up to 35W over flow rate range of 215 to 2200 ml/min. The effect of TEC cooling was also investigated for forced air convection and double-sided cooling. Experiments were also carried out to study the effect of flow rate across the heat exchanger at the bottom bay.

#### 6.6.1 Temperature Distribution Across the Thermal Test Die

To investigate the temperature distribution across the thermal test die, the temperature rise (over ambient of 21 °C) readings of the chip on the left of the second enclosure, monitored by six sets of temperature diodes described in previous section for representative test case are shown in Figure 6.14. The heat load of each chip is 20 W, and water flow rate through the heat exchanger is 5.678 l/min (1.5 gpm). Almost a uniform temperature distribution is achieved, with the highest temperature occurring at the center of the test die as expected. The variation of the distribution is about 1.3%, which indicates that the temperature at a single point is enough to characterize the chip junction temperature. Unless stated otherwise, the chip junction temperature mentioned in the following is the chip temperature monitored by the five-series of temperature diodes at the center of the package (marked by the square sign in Figure 6.14).

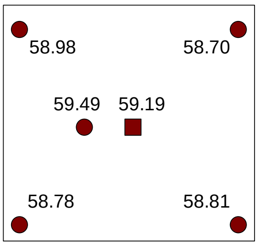



Figure 6.14 Chip temperature distributions

### 6.6.2 Single Sided Forced Air Convection Cooling (SAC) Experiments

The control valve to the micro-channel coolers is switched off so that there is no water through the micro-cooler at each chip. The heat generated within the package will primarily be dissipated through the top. Since the insulation of the test vehicle is not perfect, some heat is stored within the structure. Approximately 40 minutes are needed for the system to reach steady state for each test case.

**(1) Effect of flow rates through heat exchanger**

The effect of water flow rates through the heat exchanger at the bottom bay on the chip junction temperature was investigated under different heat loads. Three different flow rates (3.028 l/min, 5.678 l/min, and 9.464 l/min) are considered. There is no power to the TEC modules so that only forced air convection is considered. The correlation between the chip junction temperatures rise over ambient (13.5°C) and flow rates is illustrated in Figure 6.15 under chip load of 10 W. It can been seen that the chip temperature rise decreases with the increase of flow rate, with a maximum reduction of 3.5% when the water flow rate increases from 3.028 l/min to 9.464 l/min. It is found through numerical simulation that significant heat transfer (up to 430 W) occurs into the system from the ambient. The change of flow rate does not change the air temperature inside the system significantly due to this heat transfer. The effect of the water flow rate on the chip junction temperature is therefore not significant. More significant reduction of chip temperature via increasing the water flow rate is expected by using increased system insulation.

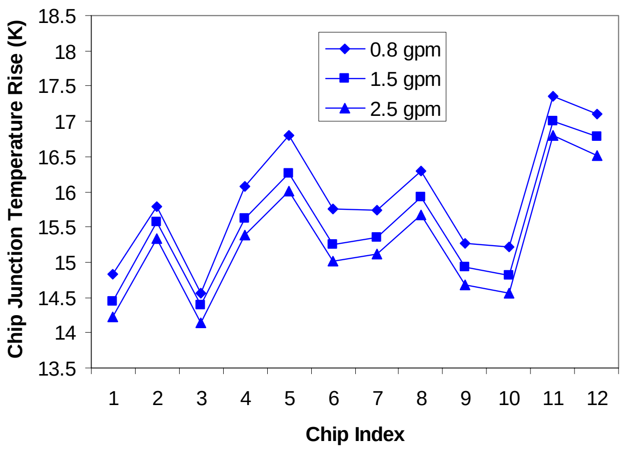



Figure 6.15 Chip junction temperature rise vs. flow rate

**(2) Effect of TEC**

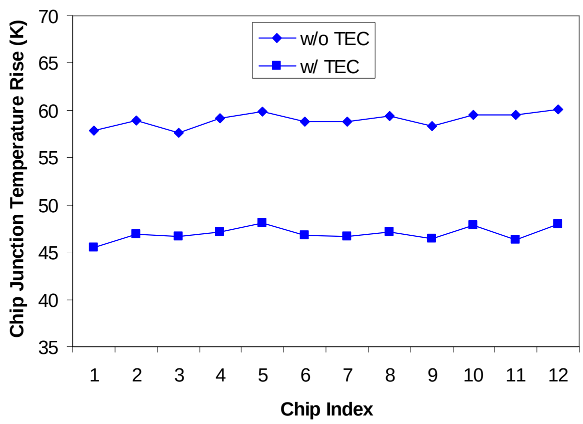



Figure 6.16 Chip junction temperature rise vs. TEC

It is interesting to investigate how much benefit the TEC modules can bring for the forced air convection cooling. The power to the TEC modules is switched on and the current to the TEC is fixed at 0.8 A. The water flow rate to the heat exchanger is 3.028 l/min (0.8 gpm), and the heat load is 20 W per chip. No water flows through the micro-cooler so that SAC is considered. Figure 6.16 depicts the chip junction temperature rise. A reduction up to 12 K or 20.4% is achieved with TEC for the current test case.

The effect of the TEC current on the heat dissipation from the package is investigated. The same test case as above is repeated for three different electric currents (0.3 A, 0.8 A, 2.0 A). Figure 6.17 shows the chip junction temperature rise. Lowest chip junction temperatures are achieved under 0.8 A, with the second lowest at 2.0 A, and only 3 °C is reduced under 0.3 A. A current of 0.2 A is insufficient to dissipate 20 W from the chip, and a current of 2.0 A is beyond for the optimal operation point of the TEC in dissipating 20 W from the chip.

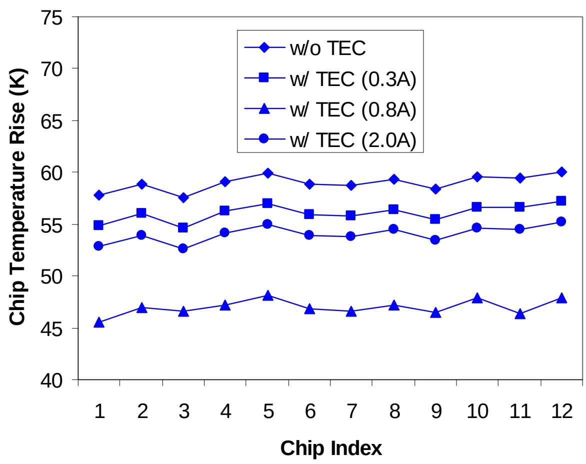



Figure 6.17 Chip junction temperature rise vs. TEC current

### 6.6.3 Single Sided Water Cooling (SWC)

The fans and blower are powered off and the control valve to the heat exchanger is switched off. The control valve to the micro-coolers is also switched off, so that the heat generation from the packages will primarily be dissipated through the bottom of the package. Since the water inlet temperature to each micro-cooler is the same, all micro-coolers are expected to have the same performance. For the demonstration, only the chip package (#9 in Figure 6.13(b)) on the left of the third enclosure is tested. The chip junction temperature rise under various flow rates is shown in Figure 6.18, from which we can see the chip junction temperature decreases with increase of the water flow rate, even though the change is not significant. The reason why the water flow rate does not affect the chip junction temperature significantly is that the thermal resistance of the micro-cooler is much smaller than the total thermal resistance of the package, which will be discussed in Chapter 7.

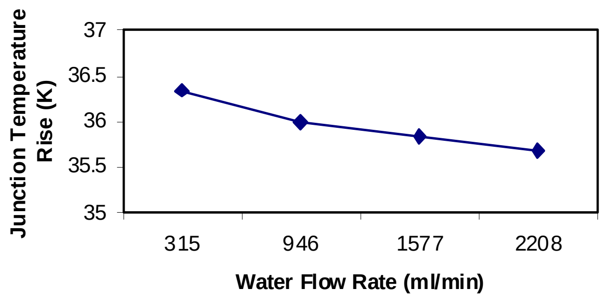



Figure 6.18 Chip junction temperature rise vs. water flow rate

### 6.6.4 Double-Sided Cooling (DSC)

Both the control valves to the heat exchanger and micro-coolers are switched on, so that the double-sided cooling takes effect. The results by DSC are compared to these by SAC and SWC under different scenarios.

**(1) Effect of double-sided cooling**

To investigate the benefit of DSC, a test case with a heat load of 20 W per chip is considered. The water flow rate through the heat exchanger is 3.028 l/min (0.8 gpm), and the water flow rate through micro-cooler is 2.208 l/min (35 gph). No TEC module is powered on for this case. The chip junction temperature rise achieved by DSC is shown in Figure 6.19. The results by SAC and SWC are also shown in the same graph for comparison. It can be seen that a reduction up to 72% in chip junction temperature is achieved with SWC, compared to SAC. The chip junction temperature is further reduced with DSC, with a reduction of 74%, compared to SAC, and 6.2% compared to SWC. Although the current benefit of DSC over SWC is not significant, e.g. only about 1 K reduction for the chip junction temperature, DSC may still be a good option when the cold water temperature is close to ambient temperature or the test vehicle is well insulated from the ambient.

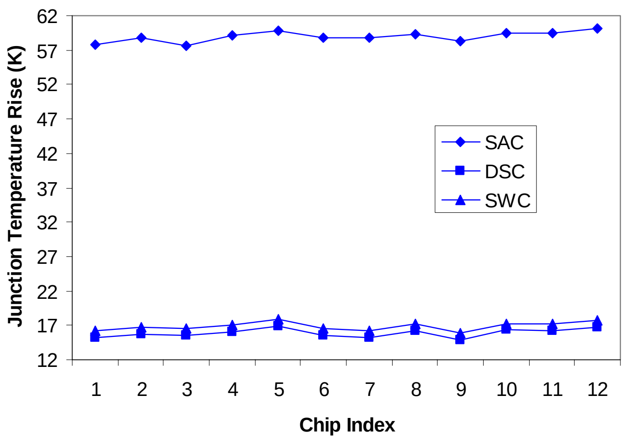



Figure 6.19 Chip junction temperature rise vs. cooling methods

### (2) Effect of TEC

The effect of TEC on double-sided cooling is also investigated. The same test case as above is conducted, except the TEC modules are powered on with an electric current of 0.8 A. Figure 6.20 shows the chip junction temperature rises with DSC when the TEC modules are switched off and on, respectively. A reduction of 0.9 K is achieved when the TEC modules are switched on. A further reduction is possible for an optimal operating current to the TEC modules.

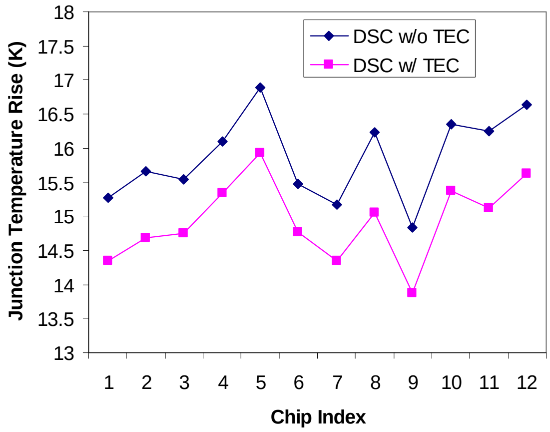


Figure 6.20 Chip junction temperature rise of DSC vs. TEC

### 6.6.5 Transient Test

A transient test was conducted for the third enclosure (③ in Figure 6.13(b)). The ambient air enters the enclosure, and flows across the three packages and exits the enclosure through the two exhaust fans. The chip packages are initially at ambient temperature (21.5 °C). The chip temperatures initially at ambient are monitored when the fans and chips are powered on (20 W/chip). For the demonstration, only SAC with TEC was investigated during this test. The current to the TEC modules is set at 0.8 A. Figure 6.21 depicts the chip junction temperature variation over time. The system reaches steady state after 150 seconds.

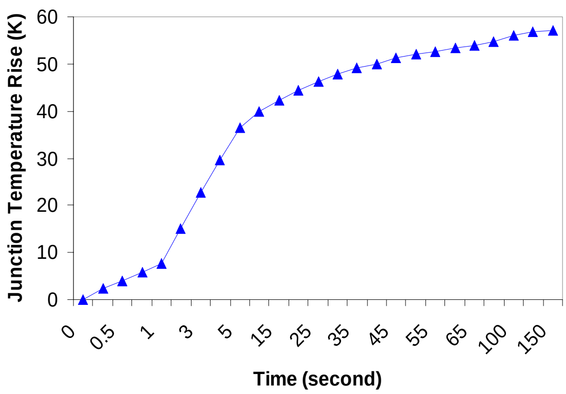


Figure 6.21 Chip junction temperature rise over time by SAC

# CHAPTER 7

# THERMAL MODELING OF TEST VEHICLE

Numerical simulations were performed to study the thermal performance of the test vehicle described in previous chapter. Compact numerical models for the key components inside the system are developed and verified by the experiments. System level simulations are conducted by replacing detailed component models with their compact models. Reduced order modeling is conducted at the system level, and the results are compared to the system level CFD simulations and experiments.

## 7.1 Multiscale Thermal Modeling Methodology

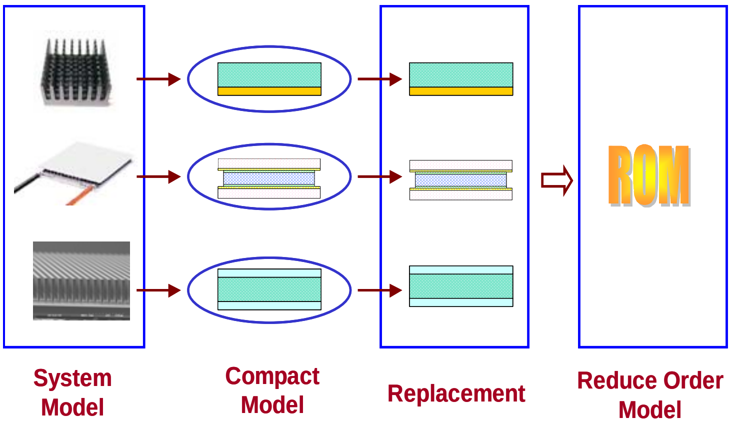



Figure 7.1 Multiscale thermal modeling methodology

Since microchannel cooler and other complex components such as heat sink, TEC, and liquid heat exchanger with small length scales are involved in the system illustrated in Figure 7.2(a), the number of grid cells of such a system model will be too large to be solved with direct numerical modeling. A feasible way to solve this problem is to develop compact models for those components, which are then utilized in the system level simulation. The POD based reduced order modeling can then be conducted at the system level. The general methodology is depicted in Figure 7.1.

### 7.2 Compact Modeling of Components

#### 7.2.1 Compact Modeling of Heat Sink

Porous medium model has been intensively studied to model air-cooled heat sinks [30, 31]. The idea of porous medium model of a parallel plate heat sink can be seen from Figure 7.2, in which the heat sink is modeled as a base plate and a prismatic block.

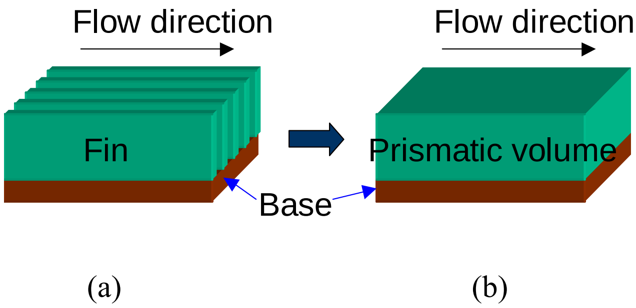



Figure 7.2 Parallel plate heat sink, (a) detailed model, (b) porous medium model

The momentum equation in a porous medium under laminar flow condition is given by [101]:

$$\frac{\partial u_i}{\partial t} + u_j \frac{\partial u_i}{\partial x_j} = -\frac{1}{\rho}\frac{\partial p}{\partial x_i} + \nu \frac{\partial^2 u_i}{\partial x_j^2} - \frac{\nu\varepsilon}{K} u_i - \frac{C_E}{K^{1/2}} u_i^2 \tag{7.1}$$

Where $K$ is the permeability of the porous metrix, ε is the porosity (see Appendix D for details), and $Ce$ is the Ergun constant. The last two terms in Equation (7.1) are typically taken as the 'linear' pressure loss and the 'quadratic' pressure loss, respectively, in CFD software packages such as Fluent or Icepak, yielding

$$\frac{\partial u_i}{\partial t} + u_j \frac{\partial u_i}{\partial x_j} = -\frac{1}{\rho}\frac{\partial P}{\partial x_i} + \nu \frac{\partial^2 u_i}{\partial x_j^2} + C_1 u_i + C_2 u_i^2 \tag{7.2}$$

where $C_1$ and $C_2$ are the linear and quadratic loss coefficients. The linear loss component results from viscous losses, which dominate at low flow velocities, whereas the quadratic loss component corresponds to the inertial loss dominating at higher velocities. The loss coefficients can be either obtained by CFD simulation, or estimated from analytical solutions for sampler configurations. Here, the CFD simulations are used to obtain the pressure drop across the detailed heat sink under various flow rates or velocities. The flow resistance imposed on the incoming flow by the heat sink fin array is described as

$$\Delta P = C_1 \frac{1}{2} \rho V_{app} + C_2 \frac{1}{2} \rho V_{app}^2 \tag{7.3}$$

Where $V_{app}$ is the approach velocity. The loss coefficients $C_1$ and $C_2$ can be obtained through curve fitting of the correlation between $\Delta P$ and $V_{app}$. The next step is to calculate $V_{app}$ for porous medium, which depends on the porosity ε

$$V_{app} = \frac{\dot{m}}{\rho A \varepsilon} \tag{7.4}$$

The energy equation for porous medium is very similar to the energy equation for a fluid, except it uses an effective thermal conductivity $\kappa_{eff}$ of the porous medium in place of the fluid conductivity

$$\frac{\partial}{\partial t}(\Phi \rho_f h_f + (1-\Phi)\rho_s h_s) + \frac{\partial}{\partial x_i}(\rho_f u_i h_f) = \frac{\partial}{\partial x_i}\left(\kappa_{eff} \frac{\partial T}{\partial x_i}\right) + \Phi \frac{DP}{Dt} + \Phi \tau_{ik} \frac{\partial u_i}{\partial x_k} \tag{7.5}$$

In Equation (7.5), $\rho_f$ and $\rho_s$ are densities of the fluid and solid phases, respectively. As derived in [30], the effective thermal conductivity of the porous block, $\kappa_{eff}$, under laminar flow can be defined as

$$\kappa_{eff} = 1.848 h_b^{3/2} (\frac{L}{\rho V_{flow}})^{3/4} \frac{\mu^{3/4}}{C_p^{1/2}} \tag{7.6}$$

where $V_{flow}$ is the mean flow velocity over the base of the compact heat sink, $h_b$ is the effective heat transfer coefficient defined as

$$h_b = \frac{Q}{A_b \Delta T_{LM}} \tag{7.7}$$

where $Q$ is the heat source, $A_b$ is the heat sink base surface area and $\Delta T_{LM}$ is the logarithmic mean temperature difference defined as

$$\Delta T_{LM} = (T_{in} - T_{out}) / \ln\left(\frac{T_b - T_{out}}{T_b - T_{in}}\right) \tag{7.8}$$

where $T_b$ is the micro-cooler base temperature, $T_{in}$ is the approaching air temperature fixed at 298.15K in this case, and $T_{out}$ is the air temperature exiting the heat sink, which can be calculated from the heat balance relationship

$$Q = \dot{m} C_p (T_{out} - T_{in}) \tag{7.9}$$

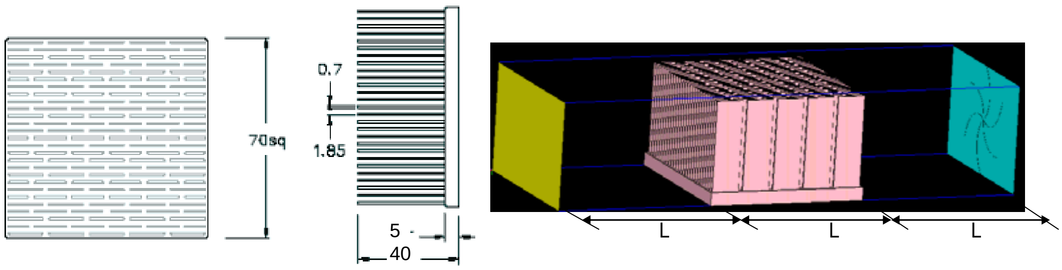
where $\dot{m}$ is the mass flow rate of the air across the heat ink and $C_p$ is the specific heat of air. For turbulent flow, the Nusselt Number of external flow over a plate under isothermal condition is [31]

$$\overline{Nu_L} = 0.0296 \mathrm{Re}_L^{4/5} \mathrm{Pr}^{1/3} \tag{7.10}$$

from which the effective thermal conductivity of the porous block can be derived as

$$\kappa_{eff} = 196.364 h_b^{3/2} (\frac{L^{1/4}}{\rho V_{flow}})^{6/5} \frac{\mu^{7/10}}{C_p^{1/2}} \tag{7.11}$$

The geometry of this heat sink under investigation is shown in Figure 7.3(a), and the corresponding numerical model with vent is depicted in Figure 7.3(b). Significant reductions (two orders of magnitude) in mesh count relative to the detailed models were achieved using the compact models, at both component level and system level, as tabulated in Table 7.1. A significant improvement (one order of magnitude) is also achieved for computational time for the heat sink under investigation.




(a) (b)

Figure 7.3 (a) dimension of heat sink (mm), (b) numerical model of heat sink (L=70mm)

Table 7.1 Node counts for CFD simulations

| Number of Node/Heat Sink | | Number of Nodes in System | | Solution Time of System (s) | |
|---|---|---|---|---|---|
| Detailed | Compact | Detailed | Compact | Detailed | Compact |
| 65,818 | 1,932 | 336,144 | 17,367 | 1,781 | 185 |

Note: 'Detailed' means detailed model, and 'Compact' means compact model.

Figure 7.4 shows the comparison of pressure drop and base excess temperature over ambient (298.15 K) between the detailed model and compact model over the entire range of air velocities (0.25 m/s to 2.0 m/s). Good agreement is achieved in all cases with a maximum relative error of 12% in the excess temperature (temperature rise over ambient temperature) of the heat sink base and 7.2% in the pressure drop. The maximum discrepancy occurs at high velocity conditions.  This loss in accuracy may be related to the decrease in fin efficiency, associated with the higher local heat transfer coefficients at the higher velocities [93]. The representative temperature and pressure contours at the y-middle plane along vertical direction obtained by both detailed modeling and compact modeling are illustrated in Figure 7.5, which indicate good agreement.

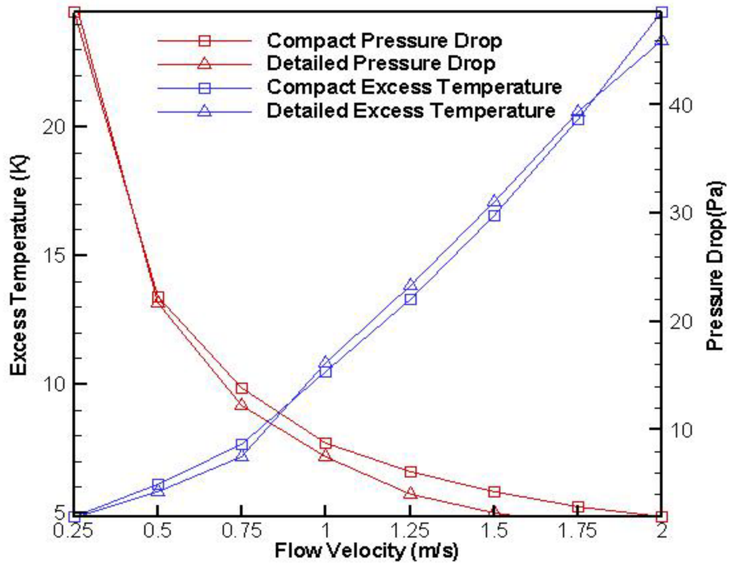
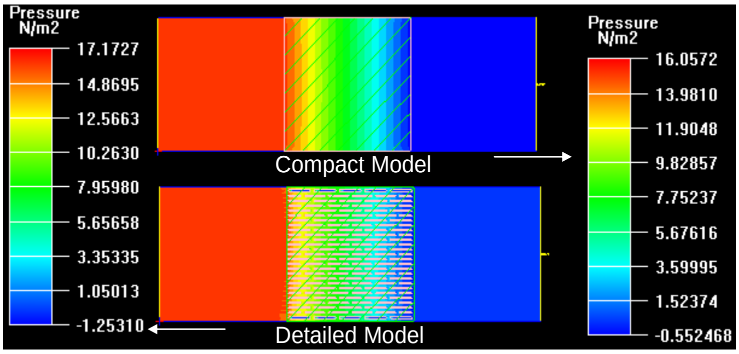
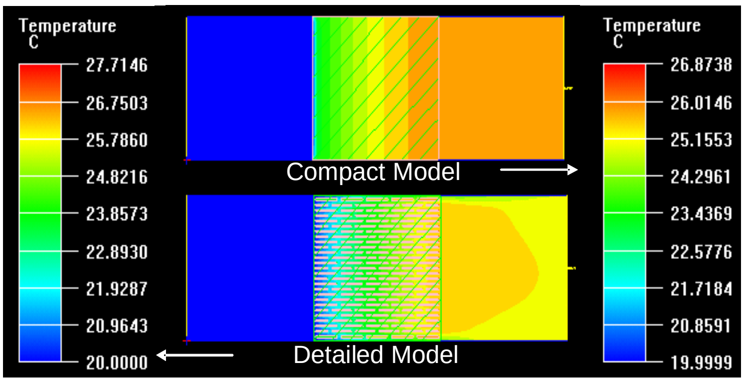



Figure 7.4 Excess temperature and pressure drop variations under Q=20 W, $V_{app}$=1 m/s.




(a)

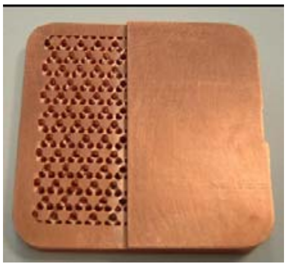



(b)

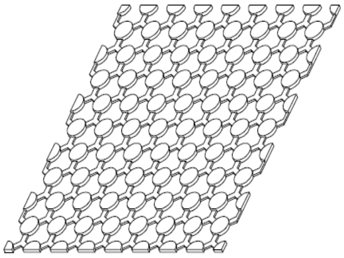
Figure 7.5 Detailed and compact model (a) pressure, (b) temperature contours at y = 0.02 m

### 7.2.2 Compact Modeling of Micro-Cooler

The physical schematic of the micro-cooler is illustrated in Figure 7.6(a), with dimensions of 48 mm (W) × 48 mm (D) × 4 mm (H). It contains ten layers of microstructure as shown in Figure 7.6(b), which are stacked together alternatively in reversed direction. Examination of the microstructure unveils that it comprises of unit cells as illustrated in Figure 6(c), from which it can been that the smallest length scale of this structure is 140 μm. Millions of grid cells will result from this small length scale for the numerical model of this micro-cooler, which means a large computational time will be required.



(a)



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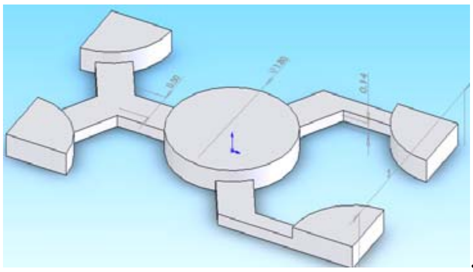
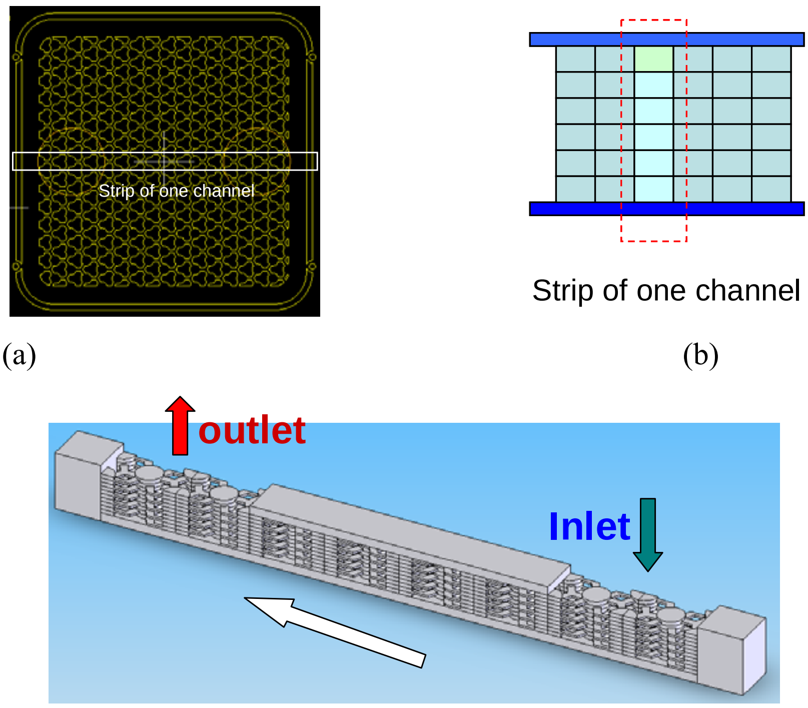


(c)

Figure 7.6 (a) physical view (b) single layer of microstructure (c) unit cell of the microstructure

To decrease the computational modeling effort, a compact model is developed by focusing on only one channel area of the micro-cooler, as shown in Figure 7.7. This model is based on the assumptions that the fluid is uniformly distributed to each channel, and heat flux across the bottom surface of the micro-cooler is also uniformly distributed. These assumptions are acceptable based on the measurement data provided by the manufacturer and the fact that highly thermally conductive pure copper is used for the entire structure.




(c)

Figure 7.7 (a) top view, (b) side view, (c) 3D compact model

The surfaces of the micro-cooler are assumed under natural convection, except the center region (10 mm × 3 mm) as the heat source with a uniform heat flux of $2 \times 10^6$ W/m$^2$. To characterize the thermal resistance of this micro-cooler, the thermal resistance is defined by

$$R_{cooler} = \frac{T_b - T_w}{Q} \tag{7.12}$$

where $T_w = (T_{w,o} - T_{w,i})/2$ is the average water temperature across the micro-cooler, $T_b$ is the top base temperature of the micro-cooler, and $Q$ is the heat dissipation by the micro-cooler. Since it is practically very difficult to get $T_b$, a total thermal resistance of the package is defined as

$$R_t = \frac{T_j - T_w}{Q} = \frac{(T_j - T_b) + (T_b - T_w)}{Q} = R_{cooler} + R_{chip} \tag{7.13}$$

where $T_j$ is the chip junction temperature, and $R_{chip}$ is the chip thermal resistance. The thermal resistance $R_{cooler}$ of the micro-cooler can be indirectly obtained once the total thermal resistance $R_t$ is obtained

$$R_{cooler} = R_t - R_{chip} \tag{7.14}$$

The chip thermal resistance can be obtained by detailed numerical simulation conducted on the package, which will be discussed later.

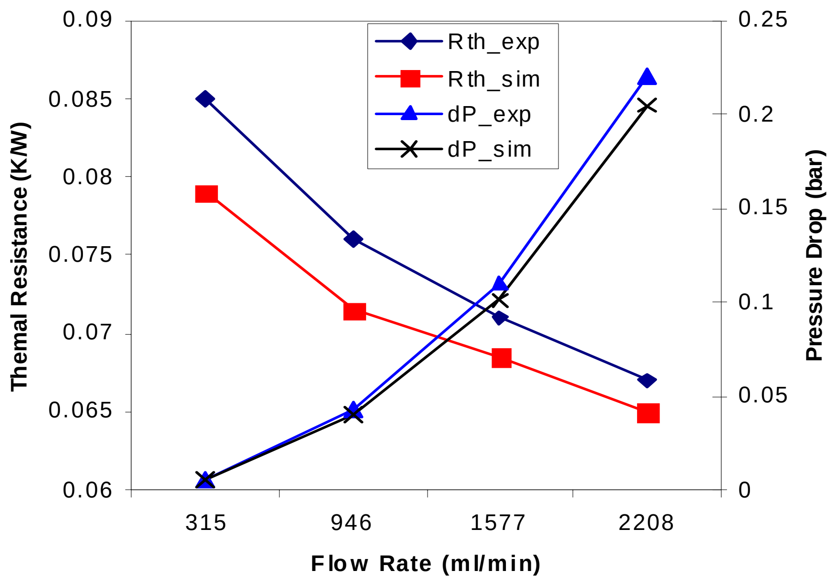



Figure 7.8 Comparison of pressure drop and thermal resistance between the compact modeling and experimental results

Figure 7.8 depicts the thermal resistances and pressure drops obtained by the experiment measurement and simulation, respectively. It can be seen that the simulated pressure drop is generally smaller than the measurements, with a difference of around 10.5%. One possible reason for the discrepancy is that the interaction, such as flow bypass between each channel, may increase the flow resistance of the system. Another possible reason could be that the fluid flow is not exactly uniformly distributed. The fluid flow along the center region may be larger than the edge region, which will result in larger pressure drop at the center region, where the measurements were conducted. The effective thermal resistances obtained by the simulation are generally somewhat smaller than the measurements, with an error up to 27.3%. Measurement and material properties uncertainty may account for this difference. It is noted that a contact thermal resistance of 0.05 K/W is assumed. An error less than 4.5% can be achieved by increasing the assumed contact thermal resistance to 0.1K/W. The package thermal resistance is calculated to be 1.26 K/W.

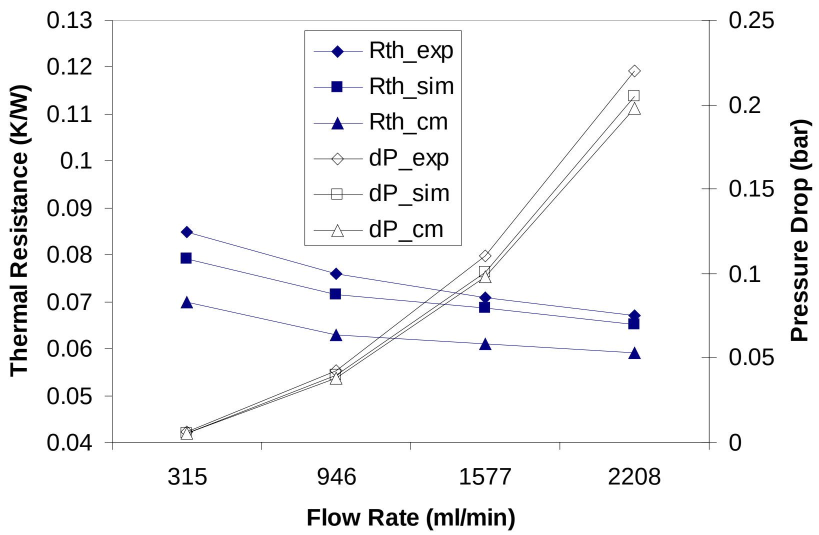
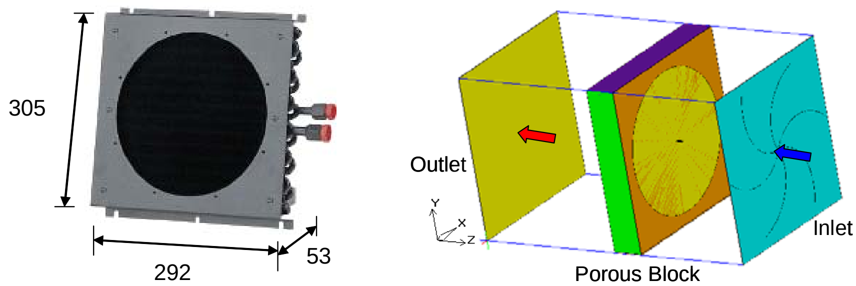



Figure 7.9 Comparison of pressure drop and thermal resistance among the 3D simulation, compact modeling and experimental results

This simplified 3D model may be a good option when the system is not very complicated. But it may be difficult to be incorporated into system level simulation of complex system, due to its large number of grid cells (1,259,848). Alternatively, a porous medium model can be developed (see Appendix D for the porosity calculation of the porous medium model of the micro-cooler). Figure 7.9 depicts the comparison among the experiments, 3D strip model, and porous medium model for the pressure drop and thermal resistance. The results for the porous medium model are lower than both the 3D strip simulation results and experimental results, with a relative error of up to 12%, compared to the experiments. This is because the porous medium model is based on the 3D strip model results, instead of the experimental results, since the simplified 3D simulation results are available in most cases. Since the results by the 3D strip model are already lower than the measurements, the porous medium modeling is expected to yield even lower results than the measurements.

### 7.2.3 Compact Modeling of Liquid-to-Air Heat Exchanger




(a) (b)

Figure 7.10 (a) schematic of heat exchanger, (b) numerical model

The schematic of the liquid-to-air heat exchanger (Lytron CP-6310) at the bottom bay of the cabinet is illustrated in Figure 7.10(a). Alternately, a porous medium model can be used to model the pressure drop of this heat exchanger, as shown in Figure 7.10(b). The loss coefficients $C_1$ and $C_2$ shown in Equation (7.3) can be obtained by curve-fitting the manufacturer's pressure drop curve under different air flow rates shown in Figure 7.11 for CP 6310. Equation (7.3) is restated here with the fitted values for $C_1$ and $C_2$:

$$dP = 3.069V_{app}^2 - 1.8059V_{app} \tag{7.15}$$

The heat transfer needs to be addressed in a different manner from the previous porous medium models for the heat sink and the micro-cooler. This is because the heat exchanger transfers the heat from the air to the water in the tubes across the entire heat exchanger domain, instead of dissipating the heat from the bottom as a heat sink does. This can be achieved by defining a vertical surface at the front or end of the porous medium with effective heat transfer coefficient and ambient temperature (mean water temperature defined as $T_w = (T_{w,o} - T_{w,i})/2$). Although the water flow in the tubes can not be modeled with this method, the heat dissipation characteristics can be fairly captured.

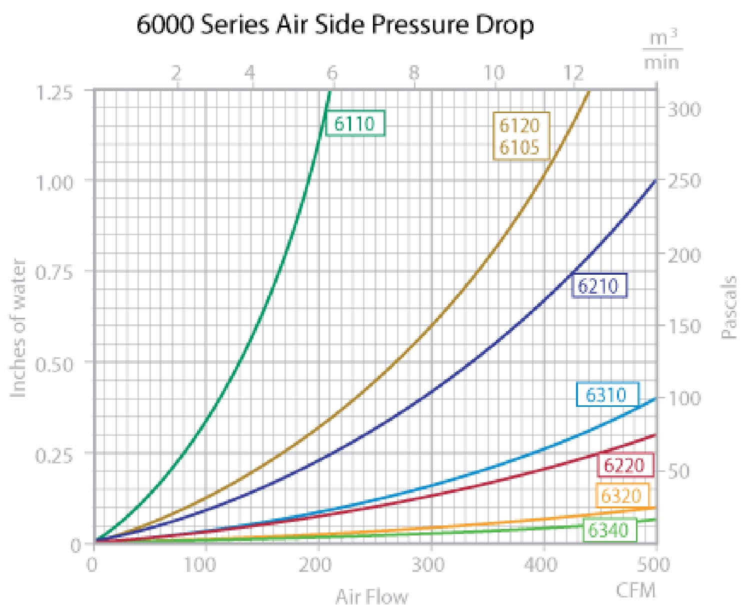



Figure 7.11 Manufacturer pressure drop vs. flow rates

The next step is to define and calculate the effective heat transfer coefficient. The heat removed by the heat exchanger can be calculated by the standard counter-flow log mean temperature difference (LMTD). LMTD is widely used to determine the temperature driving force for heat transfer in flow systems [99], as defined by

$$LMTD = \frac{Q}{F_{HX} UA_{HX}} = \frac{[(T_{a,i} - T_{w,o}) - (T_{a,o} - T_{w,i})]}{ln[((T_{a,i} - T_{w,o})/(T_{a,o} - T_{w,i})]} \tag{7.16}$$

where $T_{w,i}$, $T_{w,o}$ are the water inlet and outlet temperatures, respectively, and $T_{a,i}$, $T_{a,o}$ are the air inlet and outlet temperatures respectively. $U_{HX}$ is the overall effective heat transfer coefficient of the heat exchanger. In the current case, only the water inlet temperature and the total heat dissipation are known ($T_{w,i}$ = 8°C, Q depends on test cases). Manufacturer's thermal performance curve was used to obtain critical parameters such as $T_{a,i}$. The general procedure is shown below:

(1) Given the air flow and water flow rates, the parameter $Q/\Delta T_a$ ($=Q/(T_{a,o} - T_{w,i})$) can be obtained from Figure 7.12

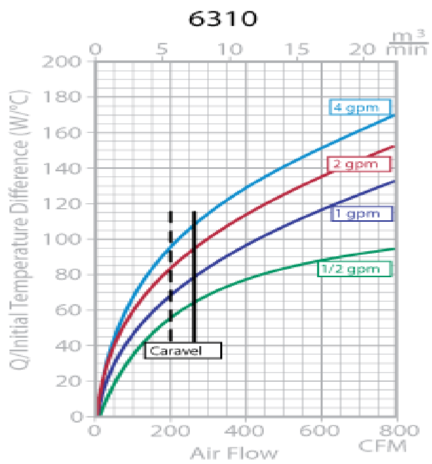



Figure 7.12 Thermal performance curve

(2) Given the heat dissipation Q, obtain $T_{a,o} = \Delta T_a + T_{w,i}$

(3) Obtain $\Delta T_a$, $\Delta T_w$ from energy balance ($Q = mc_p\Delta T_a = mc_p\Delta T_w$)

(4) Calculate $T_{a,o} = T_{a,i} - \Delta T_a$, $T_{w,o} = \Delta T_w + T_{w,I}$

(5) Calculate $U_{HX}$ from Equation (7.16). It is noted that the coefficient $F_{HX}$ is assumed to be 0.97 for current heat exchanger as suggested in [102].

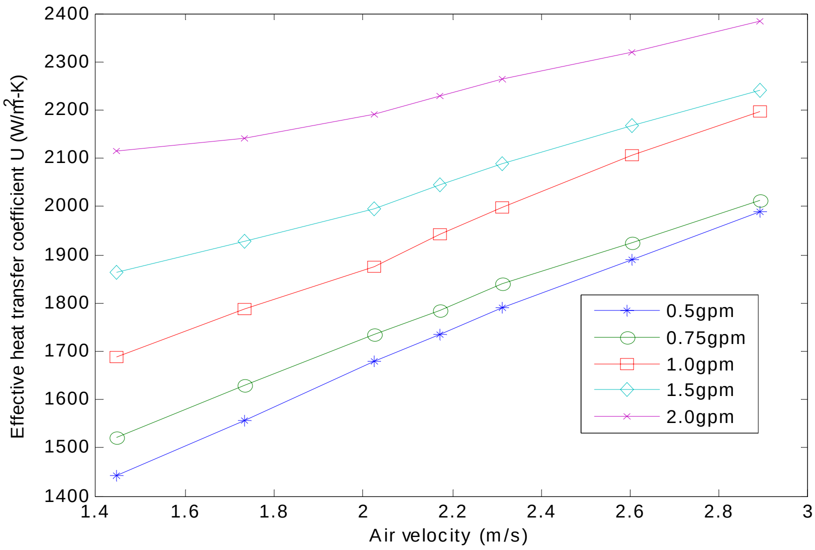



Figure 7.13 Effective heat transfer coefficient $U_{HX}$ vs. air flow rates

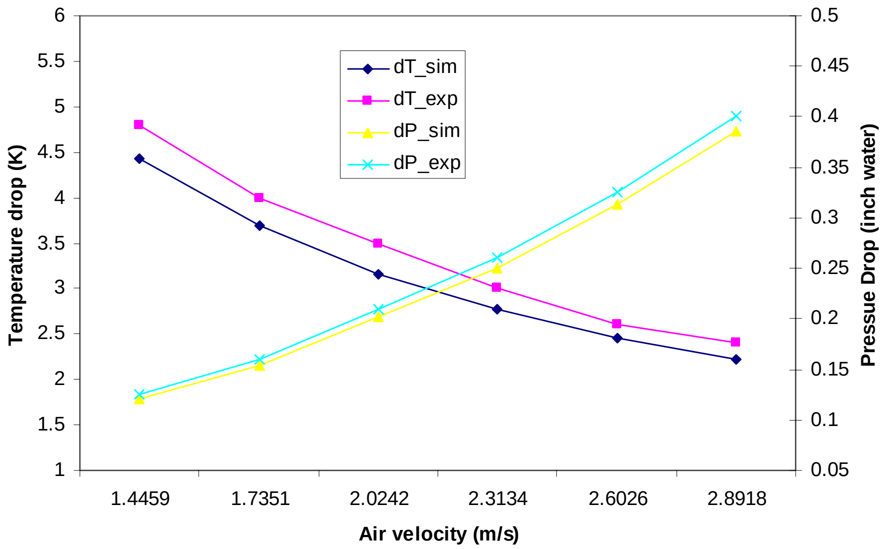



Figure 7.14 Pressure and temperature drop

The correlation of effective overall heat transfer coefficients and air flow rates under different water flow rates is depicted in Figure 7.13. It can be seen that $U_{HX}$ increases with air flow rate across the heat sink for a fixed water flow rate. The same trend holds when the water flow rate increases under a fixed air flow rate.

Figure 7.14 depicts the comparison of pressure drop and temperature decrease of the air through the heat exchanger between the simulations and measurements. An acceptable agreement is achieved under the range of all air velocities, with an approximation error of up to 10.2%. It should be noted that the pressure drop measured is taken from the manufacturer's data [103], since there are no measurements made in the test vehicle for the pressure drop.

### 7.2.4 Compact Modeling of Chip Package

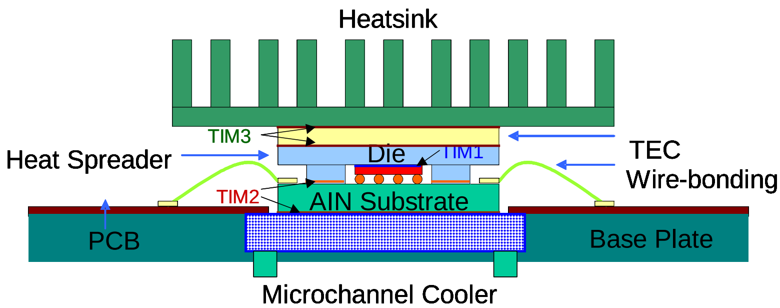



Figure 7.15 Detailed configuration of the package

Table 7.2 Geometry and thermal physical properties of package

| | Thickness (mm) | Width (mm) | κ (w/m-K) | $c_p$ (J/kg-K) | ρ (kg/m$^3$) |
|---|---|---|---|---|---|
| Die | 0.6 | 6.4 | 148 | 705 | 2330 |
| Solder | 0.2 | 6.4 | 6.0 | 160 | 7400 |
| TIM1 | 0.2 | 6.4 | 2.0 | 1000 | 2900 |
| TIM2 | 0.2 | 40 | 2.0 | 1000 | 2900 |
| TIM3 | 0.2 | 40 | 4.0 | 300 | 3000 |
| ALN | 1 | 40 | 140 | 669 | 3260 |
| Heat Spreader | 1.2 | 40 | 393 | 276 | 8960 |
| TEC | 3.3 | 40 | $\kappa_{\perp}$ =1.35, $\kappa_{//}$ =0.026 | 545 | 3766 |

The detailed configuration of the package is shown in Figure 7.15 with the geometry information shown in Table 7.2, from which we can see that the thicknesses of the TIM layers (TIM1, TIM2, and TIM3) are much smaller than other layers. It is necessary to merge these layers with other layers so that the number of the grid cells for the package, and therefore the system, will be greatly reduced.

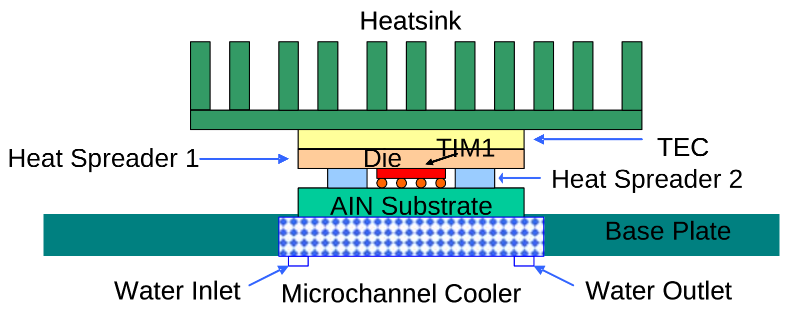
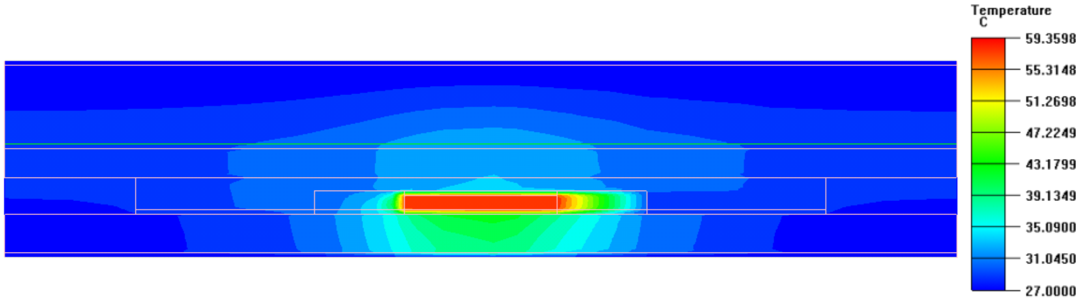



Figure 7.16 Compact model of package

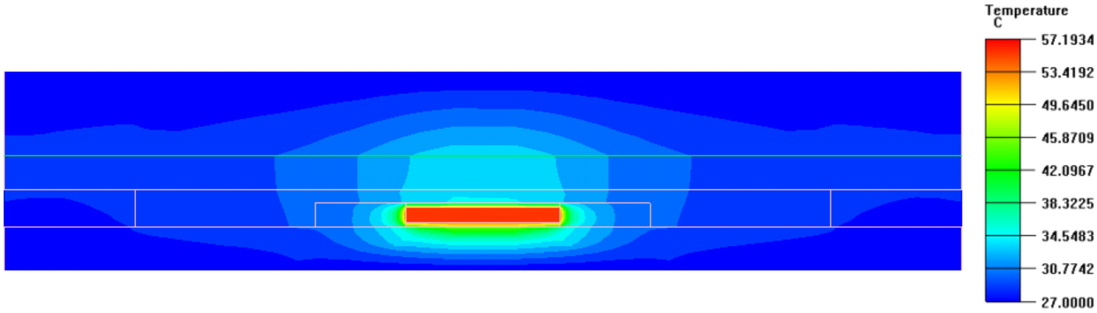
Table 7.3 Geometry and thermal physical properties of package

| | Thickness (mm) | Width (mm) | κ (W/m-K) | $c_p$ (J/kg-K) | ρ (kg/m$^3$) |
|---|---|---|---|---|---|
| Die | 1.0 | 6.4 | 148 | 705 | 2330 |
| ALN | 1 | 40 | $\kappa_{\perp}$=13, $\kappa_{//}$=134 | 600 | 3200 |
| Solder | 0.2 | 6.4 | 6.0 | 160 | 7400 |
| TIM2 | 0.2 | 40 | 2.0 | 1000 | 2900 |
| Heat Spreader 1 | 1.2 | 40 | $\kappa_{\perp}$=393, $\kappa_{//}$=314.4 | 277.3 | 8109 |
| Heat Spreader 2 | 1.2 | 40 | $\kappa_{\perp}$=410, $\kappa_{//}$=287 | 290 | 8950 |
| TEC | 3.3 | 40 | $\kappa_{\perp}$=1.46, $\kappa_{//}$=0.03 | 533.7 | 3722 |

Using the same method as described in Chapter 4 for the transient simulation, a multi-layer compact model is developed for the package, as shown in Figure 7.16. The corresponding geometry and thermophysical properties of the compact models are shown in Table 7.3. It is noted that the previous multi-layer compact model of TEC is further simplified into a single layer here. The top TIM3 layer is merged into the TEC layer, and the bottom TIM3 layer is merged into the cover of the heat spreader, which is called heat spreader 1. Part of TIM2 layer is merged into the square ring part of the heat spreader, which is called heat spreader 2. The PCB board layer has been removed, since the majority of the heat is expected to transfer through the heat sink and micro-cooler. It is noted that the TIM1 and solder layers remain in the compact model, so that the best approximation for the entire package can be achieved. Further compactization is possible if only chip junction temperature is needed during the simulation.




(a)




(b)

Figure 7.17 Temperature contour at z-middle plane, (a) detailed model, (b) compact model

Figure 7.17 depicts the temperature contours at the z-middle plane (in plane) achieved by the detailed modeling and compact modeling, respectively, under steady state and a heat load of 50 W for the chip. Both top and bottom surface are assumed at ambient temperature (27°), and the side surfaces are assumed adiabatic. The transient temperature variation of the junction temperature obtained by detailed modeling and compact modeling are shown in Figure 7.18. It can be seen that both steady state and transient results achieved by the compact modeling are close to that by the detailed modeling, with approximation error of 5.7%, which indicates that the compact model can be used for system level simulation.

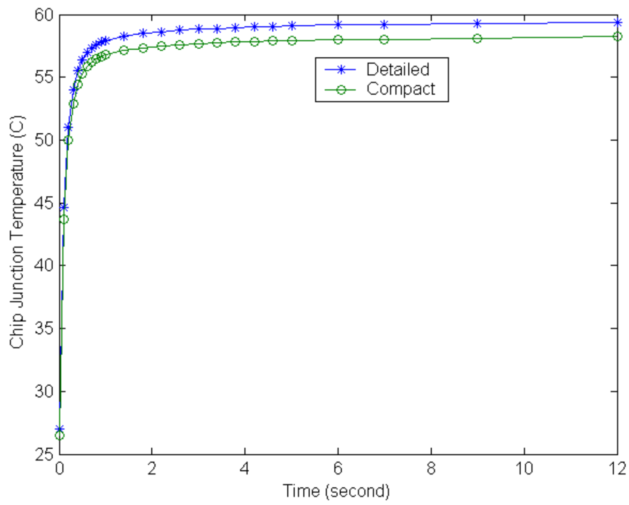



Figure 7.18 Junction temperature variance over time, (a) detailed model, (b) compact model

The thermal resistance of the package depends on the boundary conditions, due to its double-sided cooling characteristics. Three different boundary conditions are considered to investigate the thermal resistance of the package, as shown in Table 7.4. The thermal resistance is also divided into two parts: the thermal resistance through the bottom ($R_b$) and that through top of the package ($R_t$), whose values are also shown in Table 7.4. It can be seen that the thermal resistance through the bottom is much lower than the one corresponding to the heat dissipation path from the top, due to much lower thermal conductivities of TEC module and TIM1 layer. Alternative TIM1 materials are desired for improved benefit of double-sided cooling.

Table 7.4 Boundary conditions of package

| BC # | Top | Bottom | Sides | $R_t$ | $R_b$ |
|---|---|---|---|---|---|
| 1 | 300 K | Adiabatic | Adiabatic | 3.4 | NA |
| 2 | Adiabatic | 300 K | Adiabatic | NA | 1.26 |
| 3 | 300 K | 300 K | Adiabatic | 15.8 | 1.16 |

### 7.2.5 Fan Models

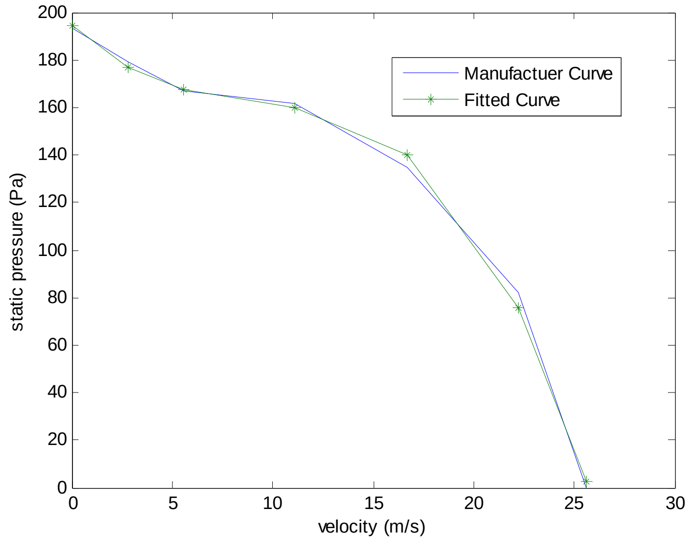



Figure 7.19 Server fan curve and polynomial interpolation

The blower at the bottom bay of the test vehicle is modeled as a cubic pressure-velocity relationship given in equation (7.17)

$$P(u) = 194.5003 - 8.4058u + 0.8183u^2 - 0.0306u^3 \tag{7.17}$$

This relationship is determined from the manufacturer's data. The comparison of the manufacturer's provided fan curve and the cubic interpolation, performed by standard regression techniques, is shown below in Figure 7.19. The computed R2 value is 0.9902 for this fit, which implies a good fit.

The same cubic interpolation of the manufacturer's data is applied to model the enclosure rack fans, resulting in the relationship given in equation (7.18)

$$P(u) = 99.0459 - 110.4486u + 98.1098u^2 - 39.7802u^3 \tag{7.18}$$

The comparison of the manufacturer's provided fan curve and the cubic interpolation is shown below in Figure 7.20. Again the fit is quite good, demonstrated by the computed $R_2$ value of 0.9886.

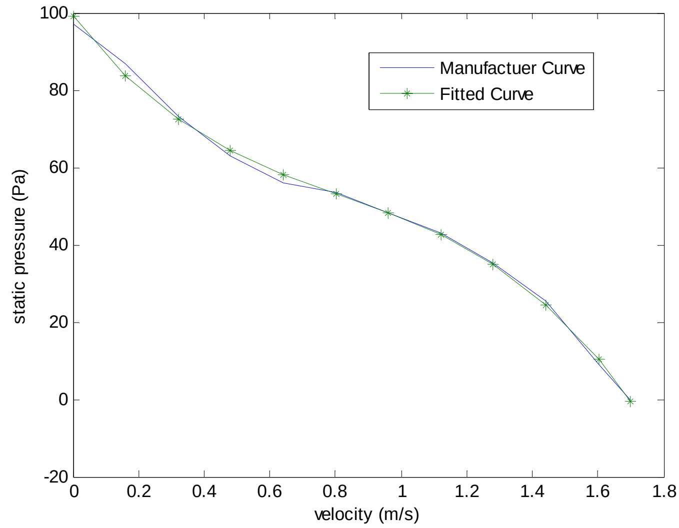



Figure 7.20 Enclosure fan curve and polynomial interpolation

### 7.3 System Level Simulation

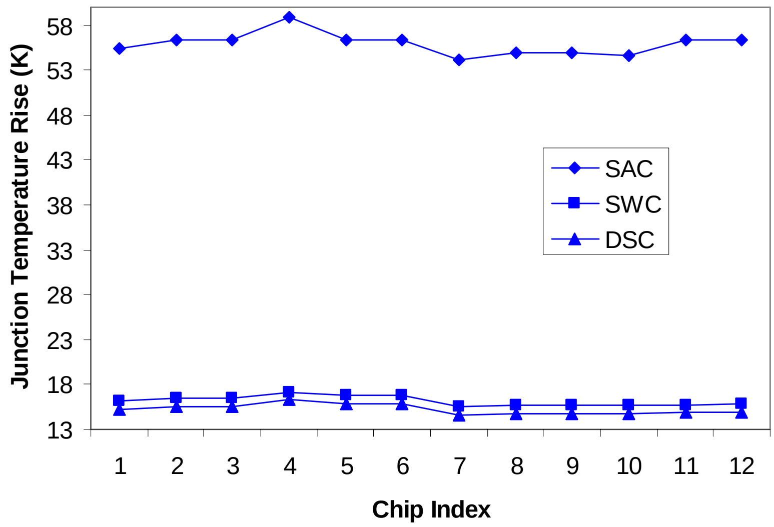
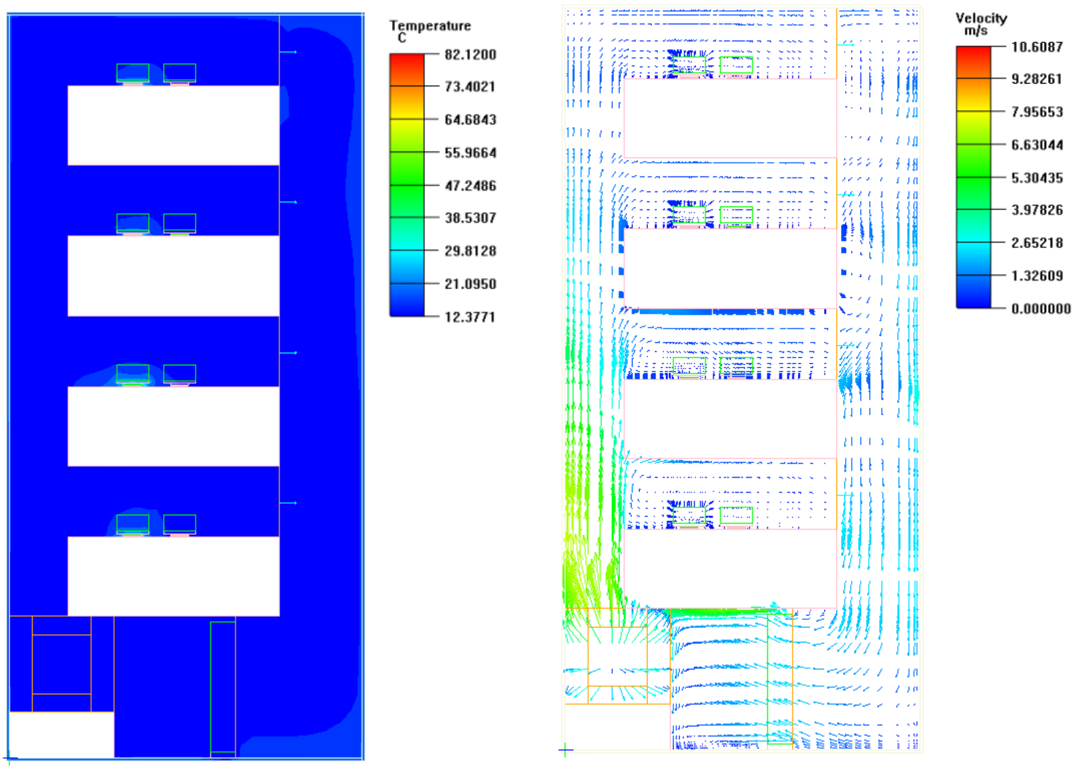



Figure 7.21 Chip junction temperature rise vs. cooling method

Once the compact model for each complex component inside the cabinet is developed, the system level simulation can be conducted by replacing these components with the compact models. Figure 7.21 depicts the chip junction temperature rises achieved by forced air convection (SAC), double-sided cooling (DSC), and water cooling

(SWC), respectively for certain representative cases. The heat load of each chip is assumed to be 20 W, and water flow rate through the heat exchanger is 3.028 l/min (0.8 gpm) and that for each micro-cooler is 2.208 l/min (35 gph). The chip junction temperature distribution is almost uniform, with the highest temperature occurring in the second enclosure and the lowest temperature occurring in the third enclosure. A reduction up to 71% for the chip junction temperatures is achieved with SWC, and a further reduction of about 1 K is achieved with DSC.

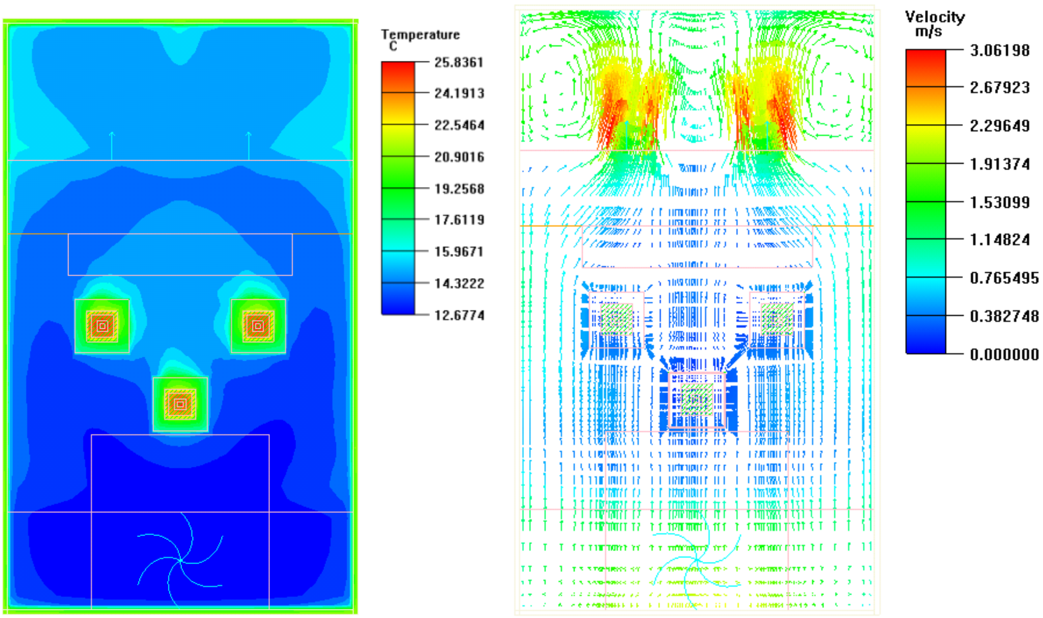
The temperature contour and velocity fields at the z-middle plane (z=0.212m) for the test case above with SSC are shown in Figure 7.22. An almost uniform velocity field for each enclosure is achieved, resulting an almost uniform temperature distribution.




(a) (b)

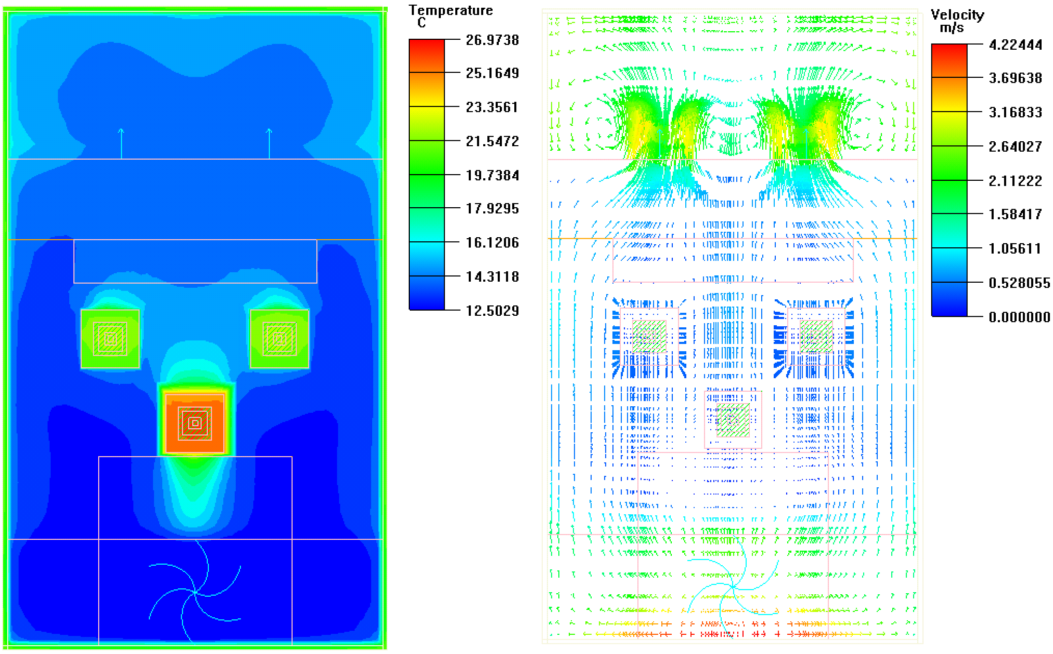
Figure 7.22 Simulation results at z-middle plane: (a) temperature contour, (b) velocity field

The temperature contours and velocity fields at the middle height of the heat sink of the second enclosure and third enclosure are shown in Figures 7.23 and 7.24, respectively. Although the air flow rate (0.0492 $m^3/s$) through the second enclosure is much higher than that (0.04482 $m^3/s$) of the third enclosure, higher chip junction temperatures are achieved for the packages within the second enclosure. The reason is that strong recirculation occurs in the second enclosure. Part of the hot air from the packages on the left and right (downstream) flows back to the first chip package (upstream), generating highest chip junction temperature (82.12°C) in this package. It is noted that the insulation of the system is not very good, since around 430 W is transferred from the ambient to the system based on the simulation. Lower chip junction temperatures are expected if better insulation layer is used.




(a) (b)

Figure 7.23 Simulation contours of the second enclosure (a) temperature, (b) velocity




(a) (b)

Figure 7.24 Simulation contours of the third enclosure (a) temperature, (b) velocity

## 7.4 Comparison of Experimental Results to the Reduced Order Modeling Results

### 7.4.1 Steady-State Test Cases

Using the same multiscale thermal modeling methodology for connected domains proposed in Chapter 4, the reduced order modeling for the test vehicle can be conducted as shown in Figure 7.25. For the demonstration, the test vehicle is decomposed into two subsystems, the top four bays and the bottom bay. Reduced order model (ROM) is developed for each subsystem, and the two ROMs are connected together to model the entire test vehicle through flow network modeling (FNM) approach (Chapter 4). It is noted that further decomposition is possible as in Chapter 4. For instance, the subsystem with top 4 enclosures can be further decomposed into one intake plenum, one exhaust plenum, and four enclosures. The procedure of modeling will remain the same.

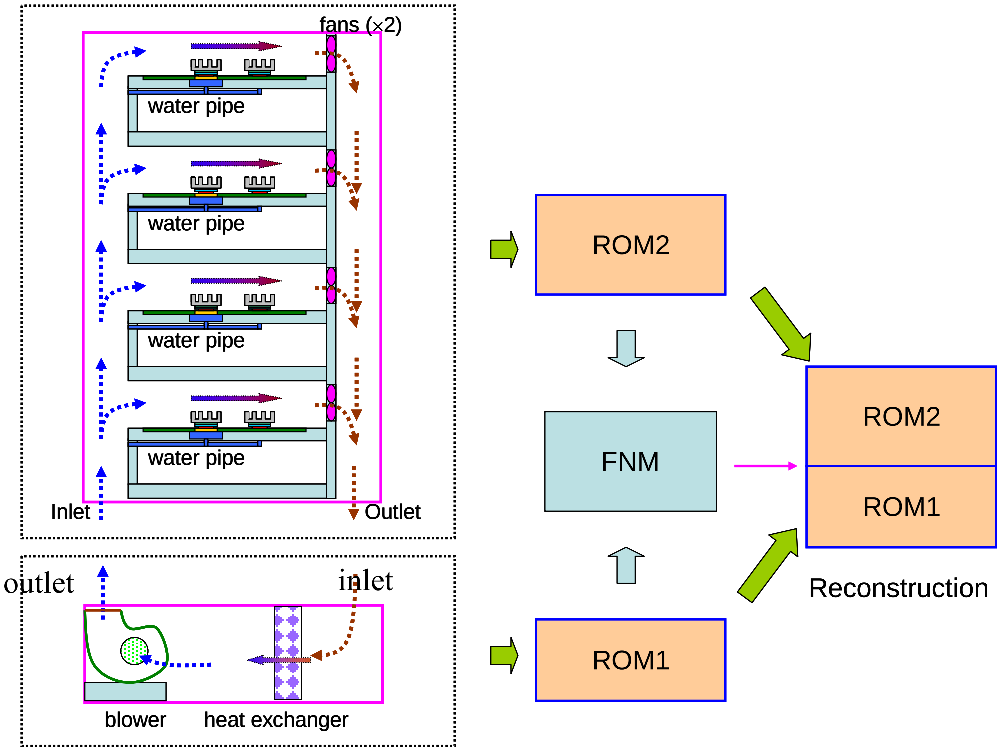



Figure 7.25 Multiscale thermal modeling of test vehicle

Table 7.5 Parameters for POD system observations

| Top ROM | | | | Bottom ROM | | |
|---|---|---|---|---|---|---|
| Snapshots | $V_{in}$ (m/s) | $Q_{chip}$ (W) | $T_{in}$ (°C) | Snapshots | $V_{in}$ (m/s) | Q (W) |
| 1 | 4.0 | 10 | 15 | 1 | 2.0 | 550 |
| 2 | 6.0 | 15 | 16 | 2 | 3.0 | 610 |
| 3 | 8.0 | 20 | 17 | 3 | 4.0 | 670 |
| 4 | 10.0 | 25 | 18 | 4 | 5.0 | 710 |
| 5 | 12.0 | 30 | 19 | 5 | 6.0 | 750 |
| 6 | 14.0 | 35 | 20 | 6 | 7.0 | 790 |
| test | 9.0 | 22 | 17.5 | test | 4.5 | 694 |

A set of 6 observations for each subsystem is generated through CFD simulation with key parameters shown in Table 7.5. As mentioned in Chapter 4, more observations may be needed for more complex flow configurations, especially in the case with fan settings of each enclosure different from each other. The outlet pressure (zero gauge pressure) is defined at the outlets of both ROMs. The heat input $Q$ to the bottom ROM is calculated by

$$Q = NQ_{chip} + Q_{ambient} \tag{7.19}$$

where $Q_{chip}$ is the chip power input, and $Q_{ambient}$ is the heat transferred to the system from the ambient. It is noted that the inlet temperature, instead of the heat input to the bottom ROM is defined during the simulation, which is calculated by

$$T_{in} = \frac{Q}{\rho V_{in} ACp} \tag{7.20}$$

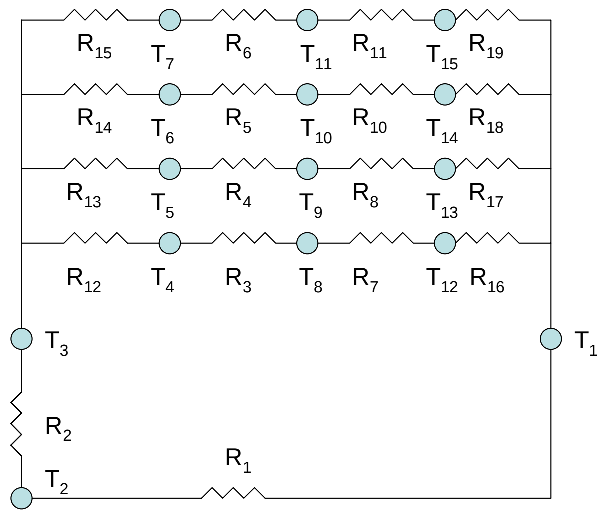



Figure 7.26 Flow resistance network of test vehicle

The flow resistance network for the system is depicted in Figure 7.26. It is noted that resistance network shown here are for the demonstration of this general approach. $R_1$ and $R_2$ are the flow resistances across the heat exchanger and blower, respectively, and $R_3$ – $R_6$ are the resistances across enclosures 1 – 4, respectively. $R_7$ – $R_{11}$ are the resistances across the fans in enclosures 1 – 4. $R_{12}$ – $R_{15}$ are the flow resistances in the intake plenum of top ROM, and $R_{16}$ – $R_{19}$ are the resistance of exhaust plenum of top ROM. The flow characteristic curve of each ROM is shown in Figure 7.27, fitted by

$$\Delta P = -3484.57\dot{V} + 20877.87\dot{V}^2 \tag{7.21}$$

where $\dot{V}$ is the volume flow rate. A minus sign is needed for bottom ROM.

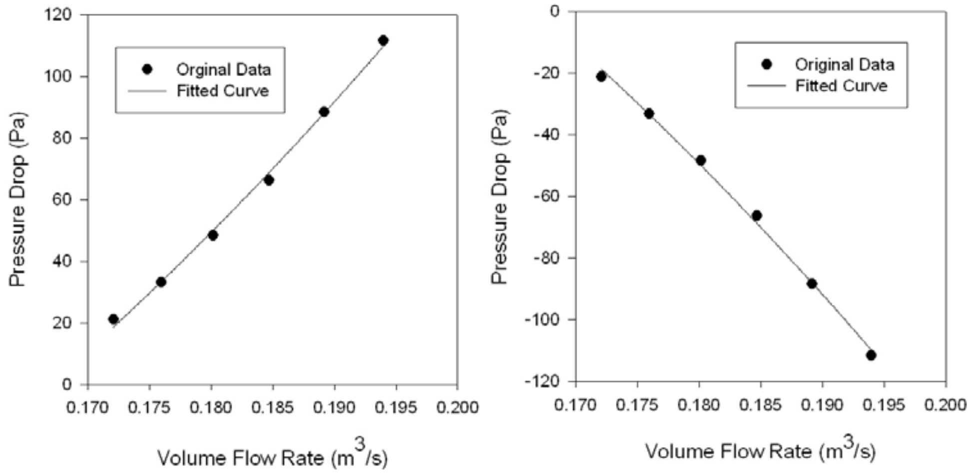



Figure 7.27 Flow characteristics of ROMs, (a) top ROM, (b) bottom ROM

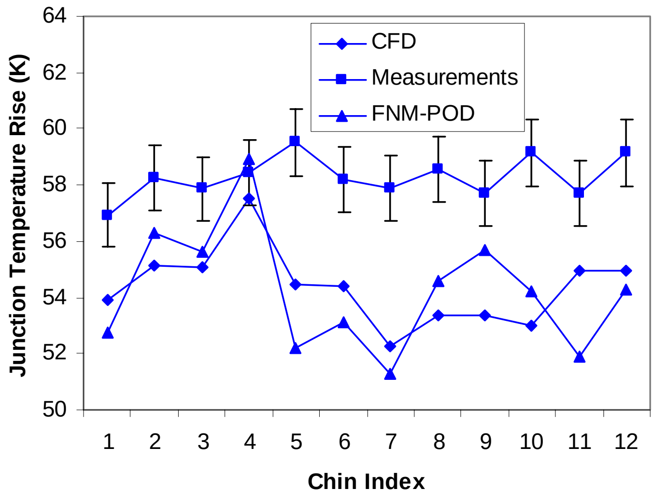



Figure 7.28 Junction temperature rise obtained by CFD, POD, and measurement

Figure 7.28 shows the chip junction temperature obtained by CFD simulations, FNM-POD based reduced order modeling, and experiment measurements, respectively. Reasonable approximation accuracy is achieved by the FNM-POD reduced order modeling, with an approximation error up to 11.2%, compared to measurement results. The errors associated with the compact modeling at component level and FNM contribute this approximation error. It is noted that the approximation error may be larger for low heat flux region, due to its relatively smaller temperature. It can be been that the chip junction temperatures predicted by CFD simulation have different trend from those measured. The reason is that the CFD simulation here includes the compact modeling for each component inside the system, and the compact modeling of each component may have different errors under different flow conditions. The same reason holds for the difference between the CFD simulations and multiscale thermal modeling results.

The DOF of the reduced system is 46 [(3×6)×2 (POD)+2×5 (FNM)], while that of CFD model is 5,949,220 (1,189,844×5), reduced by five orders of magnitude. Table 7.6 shows a complete comparison of the DOF and computational time between the CFD/HT simulation and multiscale thermal modeling. It can be seen that much less computational time (one order of magnitude less) is needed for any additional simulation by using the multiscale thermal modeling approach compared to that by CFD/HT simulation, even though much time has been spent on generating the snapshots. This renders the multiscale thermal modeling especially useful for the optimization and prototype design of electronic system, where multiple coupled simulations may need to be done.

Table 7.6 Comparison of DOF and computational time

| Types | Multiscale Thermal Modeling | CFD/HT |
|---|---|---|
| DOF of model | 46 | 5,949,220 |
| Model construction time (hours) | 4 | 4 |
| Snapshots generation time (hours) | 6×6.5=39 | NA |
| POD formation time (minutes) | 2 | NA |
| FNM solution time (minutes) | 18 | NA |
| Total run time (hours) | 43.3 | 6.5 |
| Run time for an additional case (minutes) | 20 | 390 |

### 7.4.2 Transient Test Case

A transient test case is also investigated. For the demonstration, only one enclosure (the third enclosure) is considered. The corresponding numerical model is shown in Figure 7.29. The ambient air is driven into the enclosure and exits the enclosure through the two enclosure fans. The ambient temperature is fixed to be 21.5 °C, and the chip junction temperatures are monitored once the chips and fans are powered on. The heat generation of each chip package is assumed to be 20 W, and the electrical current to the TEC is 0.8A. The water flow rate to each micro-cooler is set to be zero so that only forced air convection with TEC is simulated.

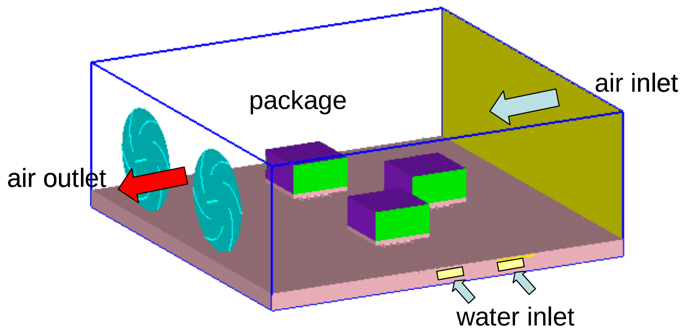



Figure 7.29 Numerical model of transient simulation

Figure 7.30 shows the variation of chip junction temperature over time obtained by compact modeling and experiment measurements. It can be seen that the general trend of the temperature variance curve by the compact modeling is close to that by the measurements, with a maximum error of 16%. Multiple reasons contribute to this discrepancy. Materials properties may not be exactly the same as those used in simulations. Secondly, compact modeling at component level may generate certain approximation errors. Thirdly, the contact thermal resistance in the heat flow path through the top of the package may not be exactly captured by numerical simulation assumptions. Also, the surface roughness and wiring of the system may increase the flow resistance. Therefore, the measured air flow rate may be lower than simulations. Finally, the measurement uncertainties may also generate non-negligible errors.

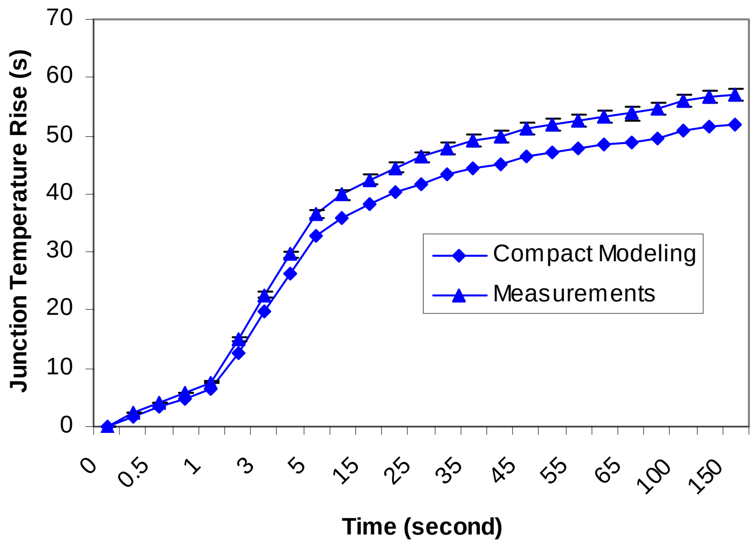



Figure 7.30 Chip temperature variance vs. time by compact modeling and measurements

# CHAPTER 8

# CONCLUDING REMARKS

## 8.1 Conclusion

a) A systematic multi-scale, multi-mode heat transfer and fluid flow modeling methodology is developed for electronic systems, such as electronic cabinets. The application of this methodology to a thermoelectrically cooled cabinet was demonstrated. A thermal modeling capability from module level (TEC module) to subsystem level (enclosure) and to system level (cabinet) has been achieved. A reduction by an order of magnitude of $10^5$ in the degrees of freedom of the system, with an approximation error less than 10% is achieved.

b) A zoom-in reduced order modeling approach was developed. This approach extended the methodology described in (a) to detailed component level simulation by extracting certain thermal information from the reduced order modeling results at system level simulation, and applying them to the detailed component model as boundary conditions. Detailed modeling across various levels is achieved through this two-step zoom-in approach. The application of the approach to a microsystem enclosure resulted in an approximation error less than 8.3% for chip junction temperature prediction under current test cases, and a reduction of two orders of magnitude for the simulation time of an additional solution.

c) A reduced order modeling methodology with boundary profile capturing capability is developed for large-scale thermal systems with pressure-driven flows. This approach significantly broadens the application of the multiscale thermal modeling methodology described above. The boundary conditions of the subsystems such as server enclosures within a complex electronic system such as an electronic cabinet are typically of unknown profile, instead of uniformly distributed variables. Serious simulation errors may be incurred without considering these boundary profile effects during the reduced order modeling at the system level. In the present work, the output profiles of the subsystem upstream are taken as the input profiles of the subsystems downstream by adding necessary flow straightening ducts during the snapshots generation process. The approximation error for the full field of velocity and pressure within a simulated server cabinet is less than 12% using this approach, and 10% for the chip junction temperature prediction, while the DOF of the system has been reduced by five orders of magnitudes.

d) An efficient coupling scheme was developed for the interconnection of multiple reduced order models of subsystems to simulate the complete system by using the concept of flow network modeling. The mass and heat flow rates, and pressure are coupled at each node of the flow resistance network using the standard SIMPLE algorithm. The coupling of mass and heat flow rates at each node is more robust and efficient than the coupling of mass and heat flux at each node, since the latter needs a very complex flow resistance network, which may result in simulation convergence problems.

e) Compact models have been developed for electronic components which can be incorporated into subsystem level and system level simulations. For example, a multi-layer compact model has been developed for thermoelectric modules with a simulation error of less than 1% for the hot side temperature of the TEC, while the number of computational nodes is reduced by 300%, compared to the detailed TEC model. A block-with-die and lead-ring compact model was developed for PQFP chip packages, with approximation error less than 8.5% for the prediction of the junction temperature under various boundary conditions. A simplified 3-D strip CFD model and a porous medium model were developed for the micro-channel cooler utilized in the test vehicle with double-sided cooling, with reasonable accuracy in predicting the pressure drop across the micro-cooler and the effective thermal resistance of the cooler, compared to the experimental results. In the meanwhile, significant reduction in the computational nodes was achieved by these simplified and compact models. Compact models were also constructed for the air-cooled heat sink and the liquid to heat exchanger, which are validated by the experiment measurements.

f) A systematic multiscale reduced order modeling approach is developed for transient thermal and fluid analysis of electronic systems. This includes the dynamic compact models for components and dynamic reduced order model for system. This approach was illustrated through an electronic enclosure with one IGBT module with four embedded IGBT devices. The dynamic multi-layer compact models were developed for IGBT devices and IGBT module by combining the detailed CFD simulation and R-C thermal circuit modeling. With the compact models for the IGBT devices and component, the dynamic reduced order model is developed for the electronic enclosure using the coefficients interpolation based POD reduced order modeling. An approximation error of 7.1% for the velocity and 9.8% for the temperature fields is achieved by the POD reduce order modeling, while the running time has been reduced from 7.5 hours to 2.5 minutes for the enclosure system under current test conditions.

g) To illustrate the application of the multiscale thermal modeling methodology under both steady state and transient scenario, a test vehicle with hybrid forced air convection, thermoelectric cooling, and micro-channel single phase liquid cooling is designed and constructed. Experiments were conducted and the results were compared to the simulation results achieved by the multiscale thermal modeling approach described above. The approximation error for the chip junction temperature rise achieved by the multiscale thermal modeling is less than 11.2% under steady state. The simulation time and DOF of the system are reduced by one order and five orders of magnitude, respectively. An error of less than 16% is achieved in the prediction of the junction temperature variation over time by the multiscale transient thermal modeling approach, compared to the experiments measurements conducted on a single enclosure of the test vehicle.

h) Experiments were conducted to compare the thermal performance of single-sided forced air convection, single-sided water cooling, and double-sided cooling for the test vehicle. The chip junction temperatures were decreased by 74% and 6.5% by double-sided cooling, compared to the single-sided air convection and single-sided water cooling, respectively. The effect of TEC on the thermal performance of the test vehicle was also studied through both experiments and simulations. The chip junction temperatures were decreased up to 20.4% when the TEC modules are switched on. The effect of the water flow rates through the heat exchanger and micro-cooler on the chip junction temperature rise was also investigated, and the results indicate that the effect is not significant, compared to the selection of cooling methods and the electrical current to the TEC modules.

### 8.2 Conclusion

a) It can be seen from the comparison between the multiscale thermal modeling and CFD/HT simulation that the reduction in computational time is not as dramatic as the reduction in the number of DOF. One reason is that the computational time for the POD based reduced order modeling defined in this work includes the time for generating POD modes and the time for obtaining weight coefficients. However, the DOF of POD based reduced order model is only defined as the number of weight coefficients. In theory, only the computational time associated with obtaining weight coefficients should be compared to the computational time of CFD/HT model. Another reason is that the number of the DOF associated with the flow network modeling is only accounted for one time during the iteration process of solving the flow network model. Another possible reason is that only matrix inversion method was used to get the weight coefficients of POD modes, while CFD/HT solvers may use more advanced solution scheme.

b) For the examples considered, the error associated with transient reduced order modeling is expected to be smaller than the steady state case when sufficient number of snapshots is generated. In general, it is hard to say which case has smaller error, since the error in reduced order modeling only depends on the number and selection of snapshots and the approach to obtain the weight coefficients.

c) The heat removal from a data center cabinet becomes more critical when it hosts advanced computing clusters containing thousands of CPUs, due to its high heat generation density. Single-phase liquid cooling, or other related cooling techniques such as spray cooling, or convective boiling may need to be utilized for the thermal management of such data center cabinets. The multiscale thermal modeling methodology developed here can be still used for the thermal analysis and design of such cabinets. Furthermore, it can be extended to larger scales, such as the entire data center that typically hosts hundreds of cabinets, as shown in Figure 3.14.

d) It is noted that the way to decompose a system into multiple subsystems is not unique. A good option is to decompose redundant parts such as server enclosures within a cabinet into subsystems. Also it is good to decompose the system based on the physical interfaces within the system such as the interfaces between the server enclosures and intake plenum and the interfaces between the server enclosures and exhaust plenum.

## 8.3 Unique Contributions

a) A systematic multi-scale, multi-mode heat transfer and fluid flow modeling methodology was developed for electronic systems, such as electronic cabinets under both steady state and transient cases.

b) A boundary capturing scheme was developed for the multi-scale thermal modeling of electronic systems.

c) An efficient coupling scheme was developed for the interconnection of multiple reduced order models of subsystems to simulate the complete system.

d) A general approach to develop multi-layer dynamic and steady compact models incorporable into system level simulation was developed.

e) Experimental validations of the multiscale thermal modeling methodology were conducted via a simulated electronic cabinet and a test vehicle with double-sided and hybrid cooling technique.

## 8.4 Recommended Future Work

a) A priori error analysis of POD modeling. Quantifying the error associated with POD models is currently an unresolved issue because the basis functions are problem-dependent, making a general theory for *a priori* error estimation very difficult. Current error analysis associated with POD modeling is focused on the *posterior* analysis [29,104,105] after the snapshots are generated and the POD modes are obtained. A priori error analysis will help to choose the optimal snapshots and the optimal number snapshots. Since the majority of the simulation time of the POD modeling is the snapshot generation, a minimum number of snapshots is very important to shorten the design and analysis time of the electronic system.

b) Transient simulation at rack level. A dynamic coupling scheme by interconnecting the dynamic ROM for each subsystem such as electronic enclosure is necessary to simulate the entire system. A dynamic flow resistance network may be needed to connect the POD based ROMs together.

c) Experimental validation of transient modeling at rack level. Experiments are necessary to validate the transient reduced order modeling at rack level using dynamic coupling scheme.

# APPENDIX A

# EFFECTIVE THERMAL CONDUCTIVITY OF COMPACT TEC MODULE

The geometries of TEC module for detailed and compact models used in simulations are shown in Figures 4(c) and 4(d), respectively. The effective thermal conductivity of the compact TEC model is derived as following:

(1) Perpendicular Conductivity

The tab and two solder layers are merged into one single layer (new tab layer) in compact TEC model. The perpendicular thermal resistance of new tab layer in compact model is calculated by

$$R_{t,cm}^{\perp} = R_{s,1}^{\perp} + R_{t}^{\perp} + R_{s,2}^{\perp} \tag{A.1}$$

where $R_{s,1}^{\perp}, R_{t}^{\perp}$, and $R_{s,2}^{\perp}$ are defined as

$$R_{s,1}^{\perp} = \frac{t_{s,1}}{\kappa_s N_{te} w_t l_t} \tag{A.2}$$

$$R_{t}^{\perp} = \frac{t_{t}}{\kappa_t N_{te} w_t l_t} \tag{A.3}$$

$$R_{s,2}^{\perp} = \frac{t_{s,2}}{2\kappa_s N_{te} w_l^2} \tag{A.4}$$

respectively. The width ($w_{t,cm}$) of new tab layer is assumed to be the same as the full width ($w_{t,f}$) of the tab layer in the detailed model, and its thickness is assumed to be the sum of the thickness of the tab and two solder layers in the detailed models, e.g.

$$t_{t,cm} = t_{s,1} + t_t + t_{s,2} \tag{A.5}$$

The effective perpendicular conductivity of new tab layer is therefore calculated by

$$k_{t,cm}^{\perp} = \left(\frac{t_{s,1}}{\kappa_s N_{te} w_t l_t} + \frac{t_t}{\kappa_t N_{te} w_t l_t} + \frac{t_{s,2}}{2\kappa_s N_{te} w_l^2}\right)^{-1} (t_{s,1} + t_t + t_{s,2}) / w_{t,f}^2 \tag{A.6}$$

For the new leg layer in the compact TEC model, its thickness remains the same as that in the detailed model. Its perpendicular thermal resistance is approximated by

$$R_{l,cm}^{\perp} = R_{l}^{\perp} \tag{A.7}$$

where the thermal resistance $R_l^{\perp}$ is defined by

$$R_l^{\perp} = \frac{t_l}{2\kappa_l N_{te} w_l^2} \tag{A.8}$$

Therefore, the effective perpendicular thermal conductivity of new leg layer is obtained by

$$\kappa_{l,cm}^{\perp} = \frac{2\kappa_l N_{te} w_l^2}{w_{t,f}^2} \tag{A.9}$$

Note that the perpendicular conductivities calculated by Equations. (A.6) and (A.9) do not account for the effect of resistance of air gaps.

(2) Lateral Conductivity

The thermal resistance of new tab layer along lateral direction is calculated by

$$R_{t,cm}^{//\;-1} = R_{s,1}^{//\;-1} + R_t^{//\;-1} + R_{s,2}^{//\;-1} \tag{A.10}$$

where each thermal resistance term is defined as

$$R_{t,cm}^{//} = \frac{1}{\kappa_{t,cm}^{//} t_{t,cm}} \tag{A.11}$$

$$R_{s,1}^{//} = \frac{2l_t}{\kappa_s w_t t_{s,1}} + \frac{(\frac{w_{t,f}}{\sqrt{(N_{te}+1)/2}} - 2l_t)}{\kappa_a w_t t_{s,1}} \tag{A.12}$$

$$R_t^{//} = \frac{2l_t}{\kappa_t w_t t_t} + \frac{(\frac{w_{t,f}}{\sqrt{(N_{te}+1)/2}} - 2l_t)}{\kappa_a w_t t_t} \tag{A.13}$$

$$R_{s,2}^{//} = \frac{1}{\kappa_s t_{s,2}} + \frac{(\frac{w_{t,f}}{2\sqrt{(N_{te}+1)/2}} - w_l)}{\kappa_a w_l t_{s,2}} \tag{A.14}$$

respectively. The effective lateral thermal conductivity of new tab layer is therefore calculated by

$$\begin{aligned}\kappa_{t,cm}^{//} = \{ & (\frac{2l_t}{\kappa_s w_t t_{s,1}} + \frac{(w_{t,f}/\sqrt{(N_{te}+1)/2} - 2l_t)}{\kappa_a w_t t_{s,1}})^{-1} + (\frac{2l_t}{\kappa_s w_t t_t} + \frac{(w_{t,f}/\sqrt{(N_{te}+1)/2} - 2l_t)}{\kappa_a w_t t_t})^{-1} \\ & + (\frac{1}{\kappa_s t_{s,2}} + \frac{(w_{t,f}/(2\sqrt{(N_{te}+1)/2}) - w_l)}{\kappa_a w_t t_{s,2}})^{-1} \} / (t_{s,1} + t_t + t_{s,2})\end{aligned} \tag{A.15}$$

For the new leg layer in the compact TEC model, its lateral thermal resistance is approximated by

$$R_{l,cm}^{//} = R_{l}^{//} \tag{A.16}$$

where each thermal resistance term is defined as

$$R_{l,cm}^{//} = \frac{1}{\kappa_{l,cm}^{//} t_l} \tag{A.17}$$

$$R_{l}^{//} = \frac{1}{\kappa_l t_l} + \frac{\left(\dfrac{w_{t,f}}{2\sqrt{(N_{te}+1)/2}} - w_l\right)}{\kappa_a w_l t_l} \tag{A.18}$$

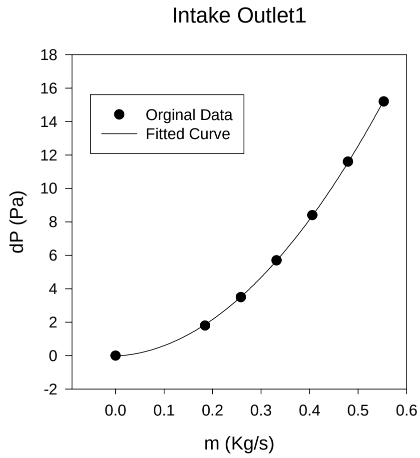
respectively. Therefore, the lateral thermal conductivity of new leg layer in the compact TEC model is calculated by

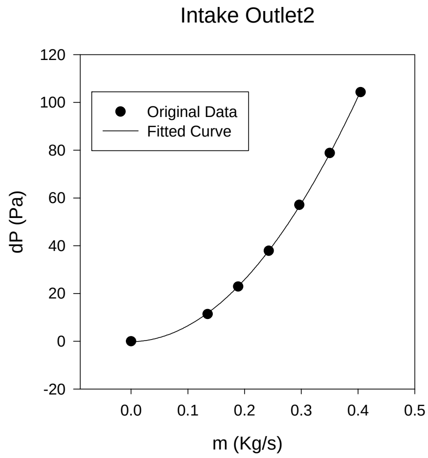
$$\kappa_{l,cm}^{//} = \left(\frac{1}{\kappa_l t_l} + \frac{\left(\dfrac{w_{t,f}}{2\sqrt{(N_{te}+1)/2}} - w_l\right)}{\kappa_a w_l t_l}\right)^{-1} / t_l \tag{A.19}$$

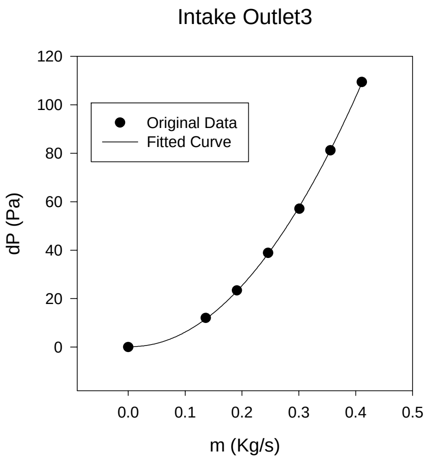
# APPENDIX B

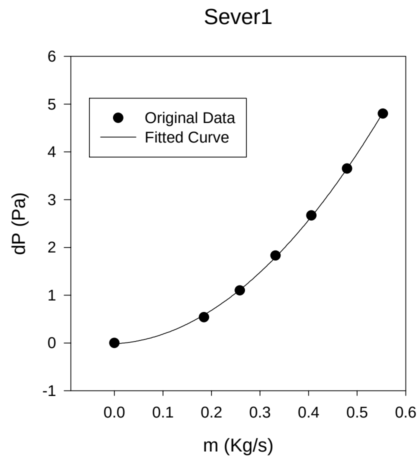
## PRESSURE DROP CHARACTERISTICS

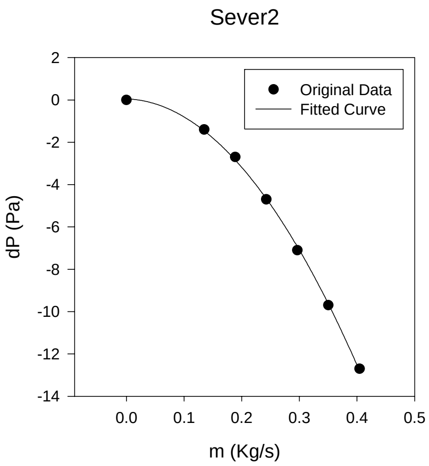
All pressure drop curves are fitted with $2^{nd}$ order polynomial for the consistence.

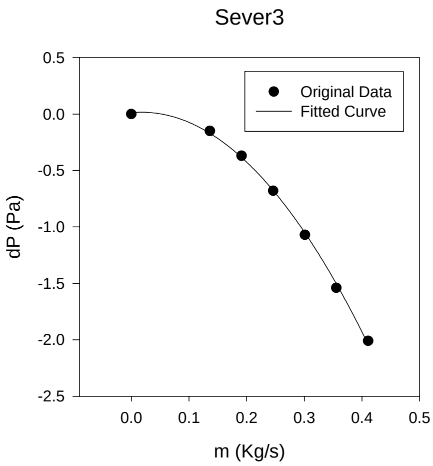


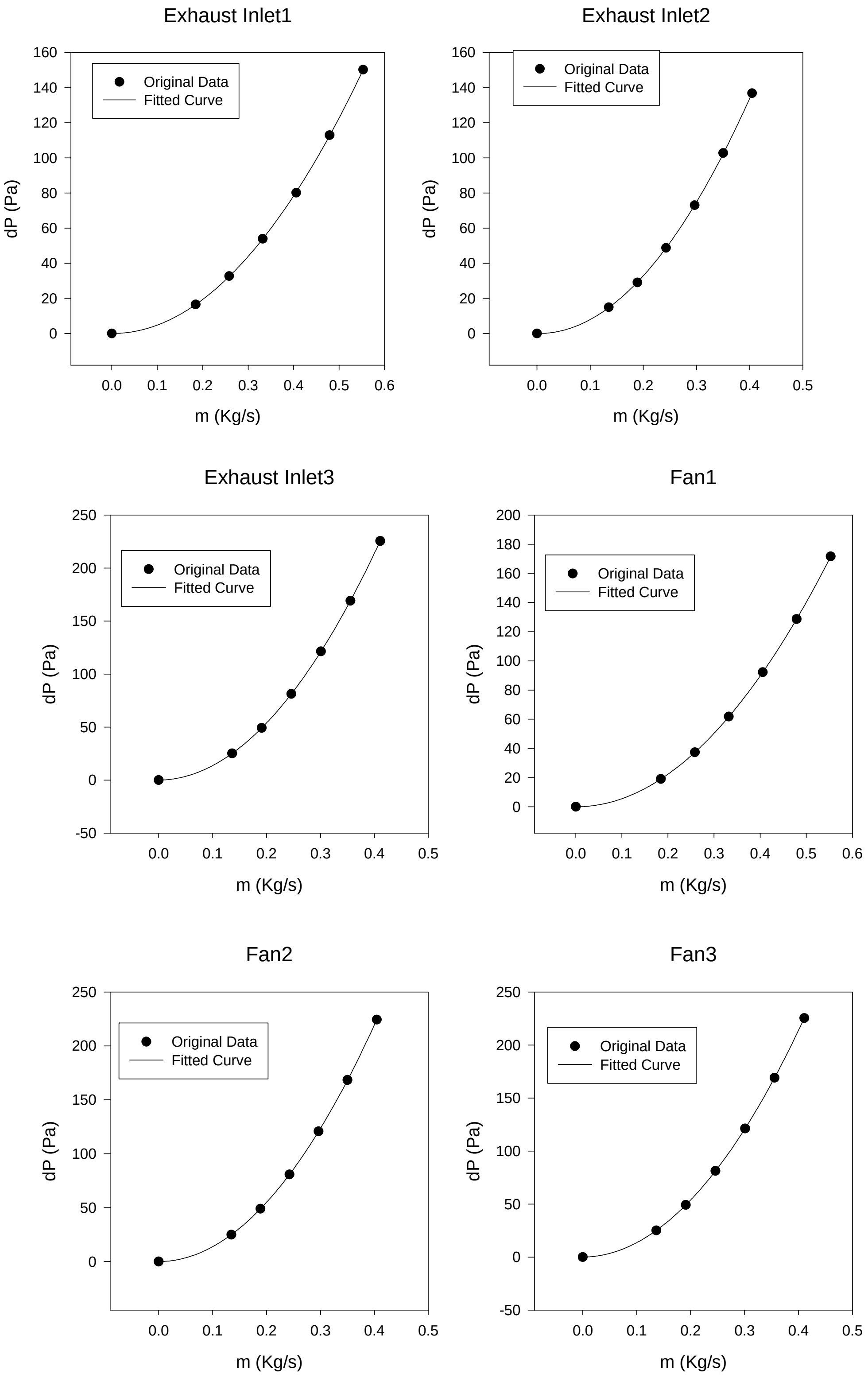



Figure B.1 Pressure characteristic curves of subcomponents

# APPENDIX C

# CALIBRATION CURVES

## C.1 Electric Resistance of Thermal Test Die

The electric resistance of heating circuit within thermal test die is designed at 20Ω. But this value may vary from die to die due to the manufacturing uncertainty and contamination. A multi-meter was used to measure the resistance $R_c$ of each heating circuit, whose values are shown in Table C.1. Since long wires are used to connect the thermal test die to the DC power supply, the external resistance also needs to be measured so that the correct voltage and current settings of the can be selected. The total resistance $R_t$ including the resistance for the thermal test die and the external resistances associated with the electric wires and solder connection are also shown in Table C.1. It can be seen that the resistance of each test die is much different. Therefore, one DC power supply is assigned to each test die so that the exact same power input to each test die can be obtained. It is noted that constant current source is recommended to power the thermal test die, since the power input of the chip can be easily obtained by measuring the total voltage across the package and wires.

Table C.1 Electric resistance

| Chip # | 1-1 (Middle) | 1-2 (Right) | 1-3 (Left) | 2-1 (Middle) | 2-2 (Right) | 2-3 (Left) |
|---|---|---|---|---|---|---|
| $R_t$ (Ω) | 19.59 | 18.52 | 22.12 | 20.99 | 22.33 | 21.08 |
| $R_c$ (Ω) | 19.81 | 18.82 | 22.12 | 21.72 | 23.10 | 21.20 |
| Chip | 3-1 (Middle) | 3-2 (Right) | 3-3 (Left) | 4-1 (Middle) | 4-2 (Right) | 4-3 (Left) |
| $R_t$ (Ω) | 18.32 | 20.68 | 22.41 | 22.45 | 22.37 | 21.08 |
| $R_c$ (Ω) | 18.45 | 21.27 | 22.93 | 23.01 | 23.04 | 22.56 |

## C.2 Thermocouple Calibration

The principal of temperature measurement of thermocouple is that a voltage will be generated at the P-N junction of the thermocouple if the temperature there is above 0 K. By finding the correlation between the temperature and the generated voltage across the junction, the temperature can be obtained once the voltage is measured. The data acquisition system typically measures the voltage across the junction of the thermocouples and outputs the temperature through the embedded algorithm on the correlation of voltage and temperature. In order to ensure the accuracy of this temperature-measurement method, an individual calibration was performed on each of the thermocouples used in experiments. Thermocouples were separately placed in a small tube of water within a thermocouple calibrator. For each of the thermocouples, the temperature of the water bath was set at 20$^{o}$C, 30$^{o}$C, 45$^{o}$C, 60$^{o}$C, 75$^{o}$C, and 90$^{o}$C [106]. The actual temperature of the water bath was indicated by a resistance temperature detector (RTD) located internally within the thermocouple calibrator. At each of the six water bath temperatures, a set of temperature measurements was taken over a two-minute interval. The time-averaged temperature found by each of the thermocouples was then compared to the RTD reading on the calibrator. Figure C.1 contains a representative result of calibration.

It was found that the maximum difference between any measured temperature and the one reported by the calibrator was approximately 0.35$^{o}$C, which is within the uncertainty of measurements. This indicates that none of the thermocouples were systematically under or over-predicting the temperatures.

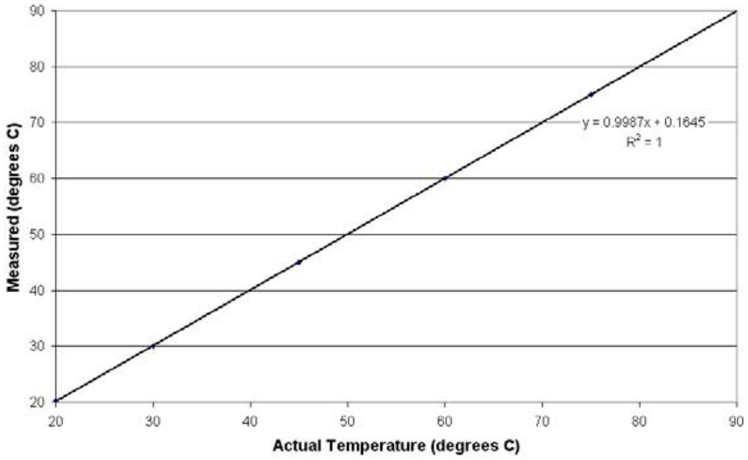



Figure C.1 Thermocouple calibration curve

### C.3 Temperature Diode Calibration

As described in Chapter 5, there are two kinds of temperature diodes within each thermal test die. For the 5-series temperature diodes, designed temperature response across one diode is 2 mV/ °C, a total of 10 mV/°C will be expected for the temperature variance of one degree with the 5 series diodes. For the bridge temperature diodes, the designed temperature response is 0.2 mV/°C. The thermal test die was placed inside an oven with embedded temperature indicator. The actual oven temperature can be accurately adjusted and read out through the indicator or calibrated thermocouple. The voltages of the temperature diodes are measured with a multi-meter. The correlations between the voltage and temperature measured by the calibrated thermocouples and oven temperature indicator are shown in Figures C.2 and C.3, respectively, for the bridge temperature diodes. From Figure C.2, a calibrated temperature response is 0.246 mV/ °C, which is larger than the designed value 0.2 mV/°C. From Figure C.3, a calibrated temperature response is 0.264 mV/°C. The first curve, which is closer to the designed value, was used in the experiments.

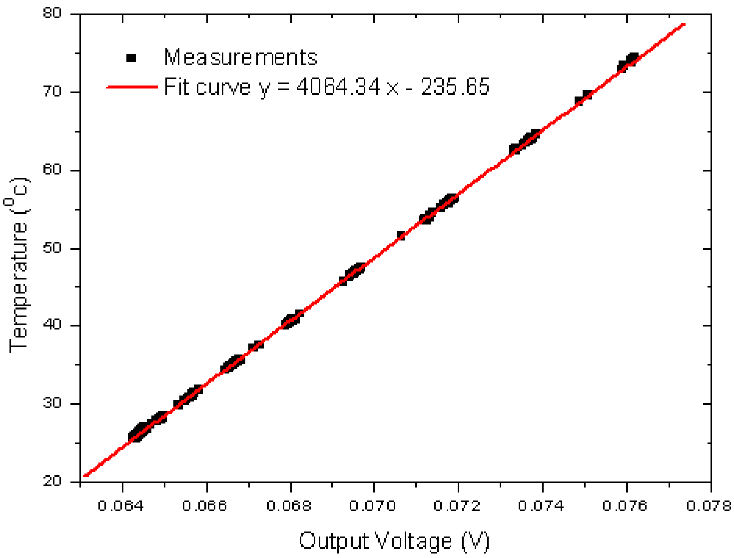



Figure C.2 Calibration curve by oven temperature indicator

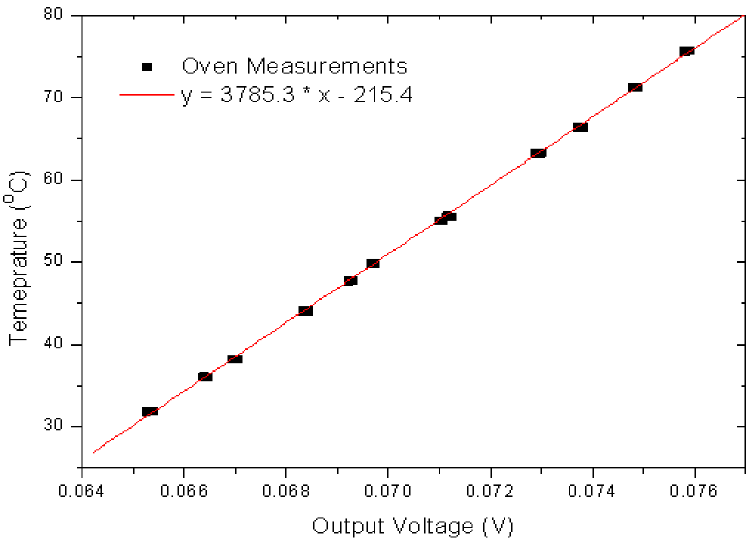



Figure C.3 Calibration curve by calibrated thermocouple

# APPENDIX D

# THERMAL TEST DIE

The outline of the thermal test die is shown in Figure D.1, with the pad information. The indexes of the pads extending outside of the outline are for the pads connected to the substrate, whose layout is shown in Figure D.2. It is noted that the temperature diodes at each corner are 5-series temperature diodes. The electric connection of each type of diodes is shown in Figure D.3. The four pads marked with $R_s$ are for power connection to the resistor in the thermal test die. The two connections from the DC power supply are connected to the two pads in diagonal direction. The five sets of 5-series temperature sensors can be connected in series so that a single DC power supply with constant current source is needed.

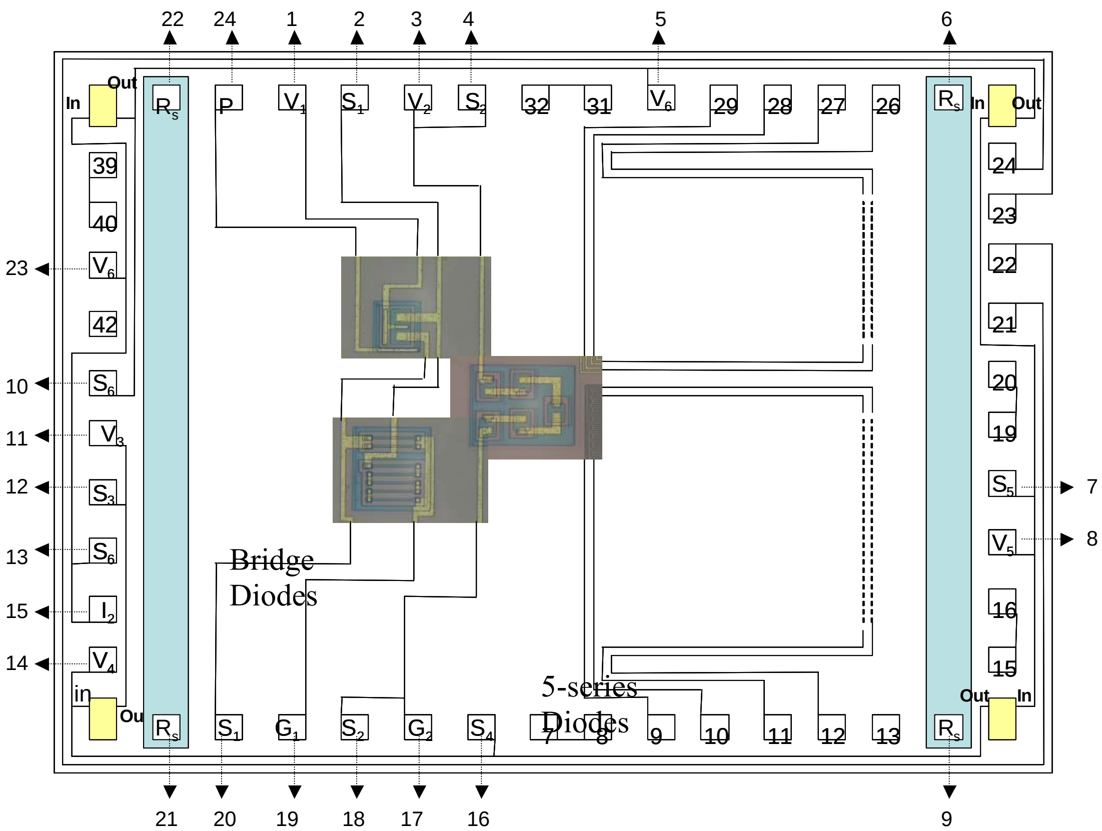



Figure D.1 Layout of the thermal test die

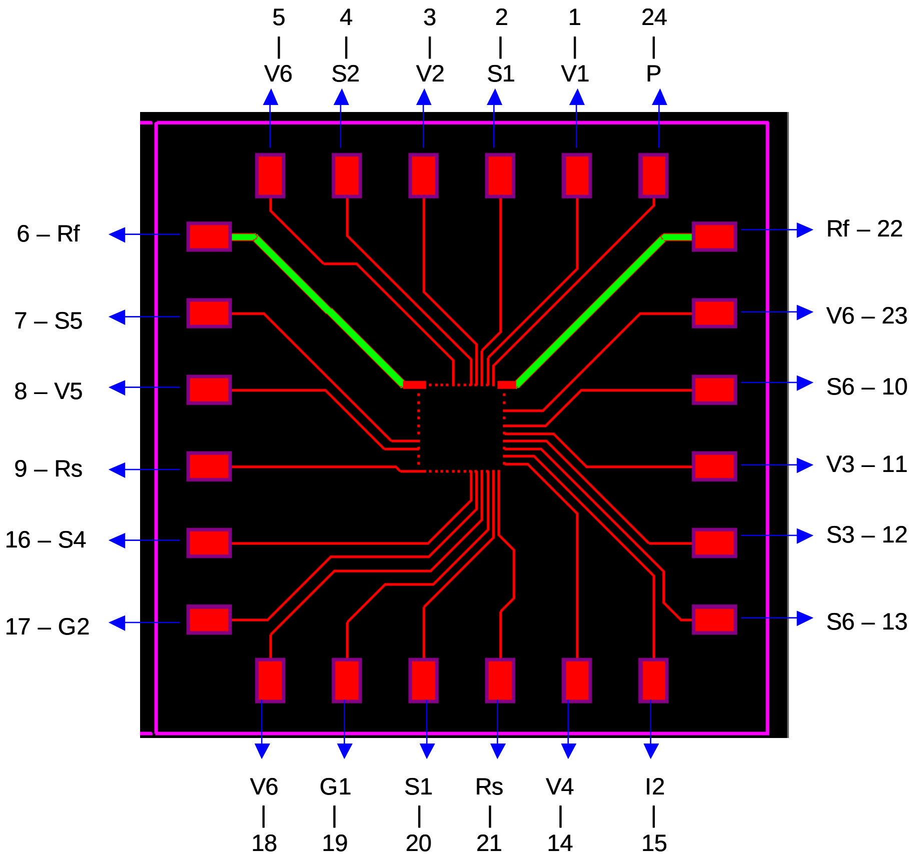



Figure D.2 Layout of the substrate

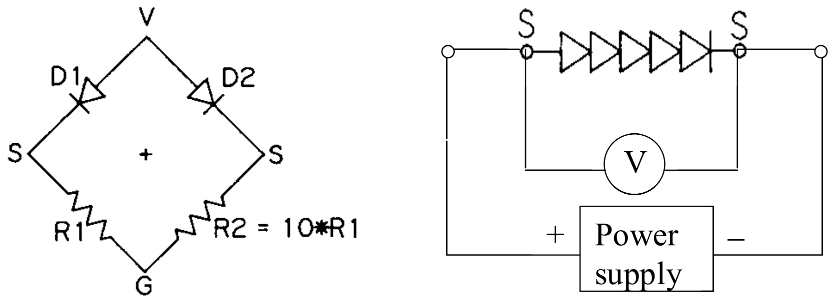



Figure D.3 Electric connection of temperature diodes: (a) bridge, (b) series

The test vehicle has four enclosures with each enclosure containing three packages. Each package has 24 electric connections, resulting a total of 288 electric connections for the entire system. A good mark for each connection is therefore necessary to avoid confusion. Figures D.4 – D.7 shows the configuration of the electric connection. Practically, all connections to the bridge temperature diodes are connected to the DC power supply in parallel and to the data acquisition system. All five sets of 5-series temperature diodes within one chip are connected to the DC power supply and data acquisition system. These connections to the series temperature diodes are switched to the next chip after the data for the first chip has been collected. Many electric wires can be saved through this switching mode. For transient measurement, all chips needs to be connected to the power supplies and data acquisition system, since all data needs to be collected at the same time.

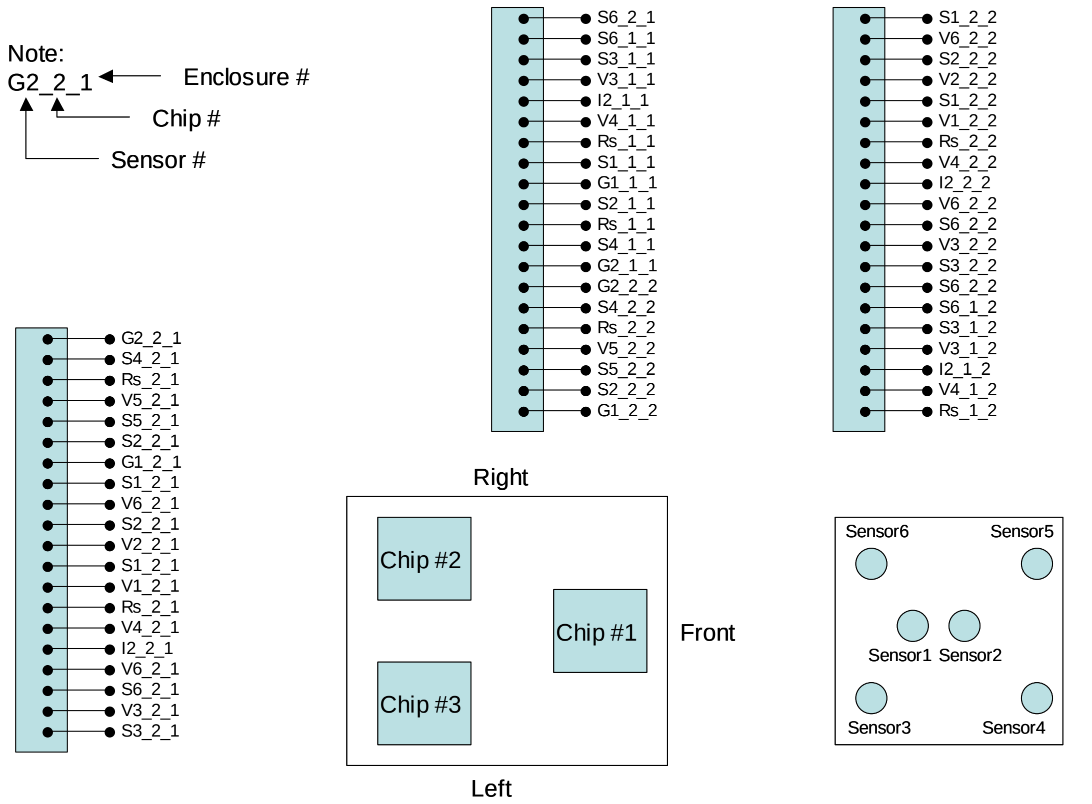



Figure D.4 The bottom half connectors at the left wall

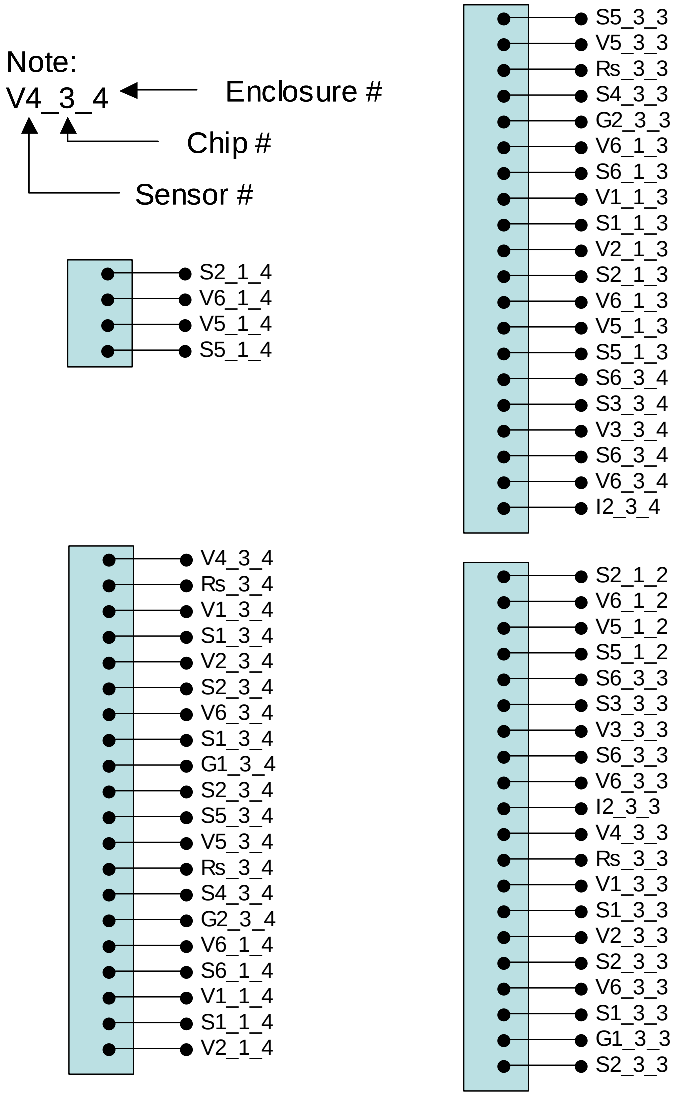



Figure D.5 The top half connectors at the left wall

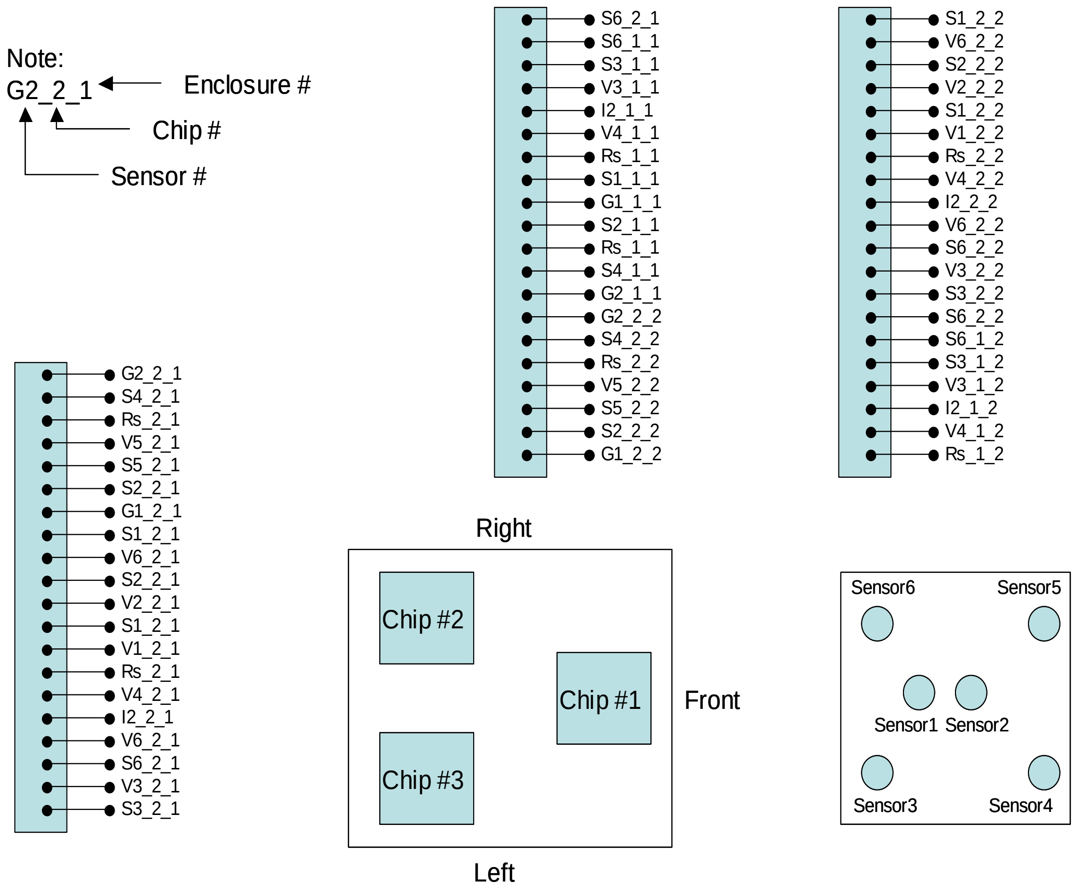



Figure D.6 The bottom half connectors at the right wall

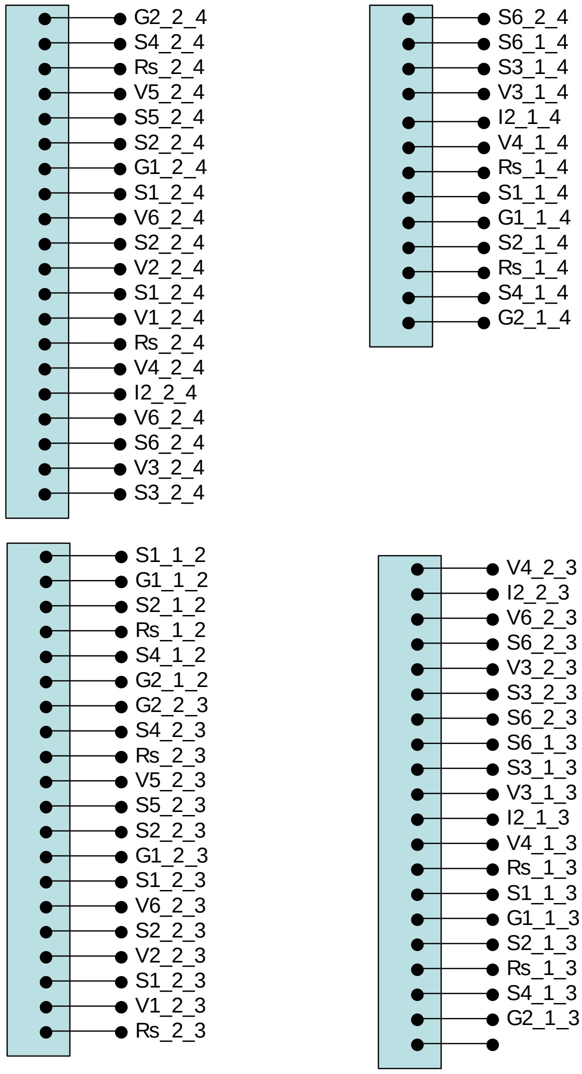



Figure D.7 The top half connectors at the right wall

# APPENDIX E

# POROUS MEDIUM MODEL

The heat sink and micro-cooler were modeled as porous medium model. The porosity and pressure loss coefficients of each model are described below.

(1) Heat sink

The geometry of the heat sink is shown in Figure E.1. The porosity ε can be calculated by

$$\varepsilon = \frac{40 \times 35 - 0.7 \times 35 \times 16}{40 \times 35} = 0.72 \tag{E.1}$$

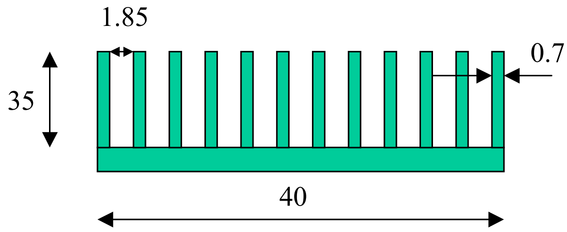



Figure E.1 Geometry of heat sink utilized in test vehicle

(2) Micro-cooler

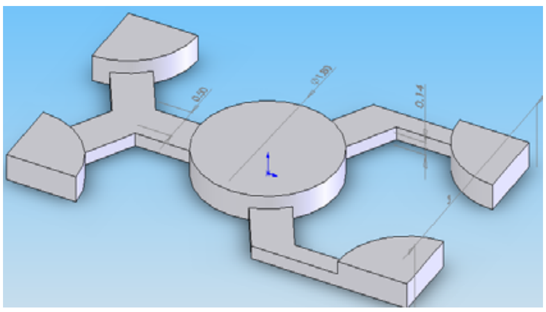


Figure E.2 Unit cell structure of micro-cooler

The geometry of the unit cell of the micro-cooler is shown in Figure E.2. The porosity ε can be calculated by

$$\varepsilon = \frac{(3 \times 5.196 - 2 \times \pi \times 0.9^2 - 0.832 \times 0.5 \times 3) \times 0.28}{3 \times 5.196 \times 0.28} = 0.557 \tag{E.1}$$

## REFERENCES


[1] "International Technology Roadmap for Semiconductors," “International Technology Roadmap for Semiconductors 2007”, http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_PIDS.pdf., [accessed June 25, 2008].

[2] D. B. Tuckerman and R. F. W. Pease, "High Performance Heat-Sinking for VLSI," *IEEE electron Device Letter* vol. 2, pp. 126-129, 1981.

[3] C. D. Patel, C. E. Bash, C. Belady, L. Stahl, and D. Sullivan, "Computational Fluid Dynamics Modeling of High Compute Density Data Centers to Assure System Inlet Air Specifications," presented at IPACK’01 -The Pacific Rim / ASME International Electronics Packaging TechnicalConference and Exhibition, Kauai, HI, 2001.

[4] "Heat Density Trends in Data Processing, Computer Systems and Telecommunications Equipment," *The Uptime Institute, available at: http://www.upsite.com/TUIpages/tuiwhite.html*, [accessed May 25, 2008].

[5] Ashrae, "Datacom Equipment Power Trends and Cooling Applications," presented at American Society of Heating, Refrigeration and Air-conditioning Engineers, Atlanta, GA, 2005.

[6] N. Rolander, "An Approach For The Robust Design of Air Cooled Data Center Server Cabinets," vol. MSME thesis. Atlanta, GA: Georgia Institute of Technology, 2005.

[7] R. E. Simons and R. C. Chu, " Application of Thermoelectric Cooling to Electronic Equipment: A Review and Analysis," presented at 16th IEEE SEMI-THERMTM Symposium, San Jose, CA, 2000.

[8] A. Latrobe, M. Cadre, and J. P. L. Jannou, "Simulation and Experimentation of Air Flow in Electronic Racks," presented at Proc. INTELEC 86, IEEE Int. Telecommun. Energy Conf., 1986.

[9] M. Cadre and A. Viault, "Thermal Simulations for Electronic Equipment Using the Software Package ‘THEBES’," presented at Proc. INTELEC 89, 11th Int.Telecommun. Energy Conf., 1989.

[10] T. Kobayashi, M. Nakamura, T. Ogushi, A. Iwamaru, and M. Fujii, "Thermal Design of a Closed Cabinet with a Heat Exchanger for Inner Air Cooling," *Heat Transfer—Asian Research*, vol. 30, pp. 267-279, 2001.

[11] T. Ogushi and G. Yamanaka, "Simulation of Natural Ventilation in Electronic Cabinet," presented at Conference Proceedings of 68th JSME, 1990.

[12] T. Kowalski and A. Radmehr, "Thermal Analysis of An Electronics Enclosure: Coupling Flow Network Modeling (FNM) and Computational Fluid Dynamics (CFD)," presented at IEEE 16th Semiconductor Thermal Measurement and Management Symposium, San Jose, CA, 2000.

[13] J. Rambo and Y. Joshi, "Reduced-order Modeling of Steady Turbulent Flows Using the POD," presented at ASME Summer Heat Transfer Conference & InterPACK'05, San Francisco, CA, 2005.

[14] J. Wei, "Thermal Management of Fujitsu's High Performance Servers," *Journal of Fujitsu Science Technology*, vol. 43, pp. 122-129, 2007.

[15] Q. Nie and Y. Joshi, "Multiscale Thermal Modeling Methodology for Thermoelectrically Cooled Electronic Cabinet," *Numerical Heat Transfer, Part A*, vol. 53, pp. 225-248, 2008.

[16] Y. Joshi, "Recent Progress and Some Challenges in Thermal Modeling of Electronic Systems," *Advances in Numerical Heat Transfer.* , vol. 2, pp. 371-406, 2000.

[17] P. S. Sathyamurthy and S. V. Patankar, "Block-correction-based Multi-grid Method for Fluid Flow Problems," *Numerical Heat Transfer, Part B*, vol. 25, pp. 375-394, 1994.

[18] T. J. Heindel, F. P. Incropera, and S. Ramadhyani, "Enhancement of Natural Convection Heat Transfer from An Array of Discrete Heat Sources," *Int. J. Heat Mass Transfer*, vol. 39, pp. 479-490, 1996.

[19] M. Wankhede, V. Khaire, and A. Goswami, "Evaluation of Cooling Solutions for Outdoor Electronics," presented at 13th International Workshop on Thermal Investigation of Ics and systems, Budapest, Hungary, 2007.

[20] R. L. Linton and D. Agonafer, "Thermal model of a PC," *Numerical Simulation of Convection in electronic Equipment Cooling, ASME, HTD-121*, pp. 69-72, 1989.

[21] C. Lasance and Y. Joshi, *Thermal Analysis of Natural Convection Electronic Systems: Status and Challenges, Advances in Thermal Modeling of Electronic Components and Systems ,Bar-Cohen, A., and Kraus, A. D., eds.*, vol. 4. New York: ASME Press/IEEE Press, 1998.

[22] R. L. Linton and D. Agonafer, "Coarse and detailed CFD modeling of a finned heat sink," presented at Proceedings of I-THERM IV, InterSociety Conference on Thermal Phenomena in Electronic Systems, Washington, D.C., 1994.

[23] L. Tang and Y. Joshi, "Integrated Thermal Analysis of Natural Convection Air Cooled Electronic Enclosure," presented at HTD-Vol. 329, National Heat Transfer Conference, Houston, Texas, 1996.

[24] V. H. Adams, D. L. Blackburn, Y. Joshi, and D. W. Berning, "Issues in Validating Packaging Compact Thermal Models for Natural Convection Cooled Electronic Systems," presented at Thirteenth IEEE Semi-ThermTM Symposium, 1997.

[25] A. Bar-Cohen and W. Krueger, "Thermal Characterization of a PLCC-Expanded Rjc Methodology," *IEEE Transactions Component Hybrid and Manufacturing Technology*, vol. 15, pp. 691-698, 1992.

[26] C. Lasance, H. Vinke, and H. Rosten, "Thermal Characterization of Electronic Devices by Means of Boundary Condition Independent Compact Models," *IEEE Trans Comp, Hybrids, and Manuf Tech*, vol. 18, pp. 723-731, 1995.

[27] V. H. Adams, Y. Joshi, and D. L. Blackburn, "Application of Compact Model Methodologies to Natural Convection Cooling of An Array of Electronic Packages in A Low Profile Enclosure," *ASME Advances in Electronic Packaging*, vol. 2, pp. 1967-1974, 1997.

[28] B. Shapiro, "Creating Reduced-Order Models for Electronic Systems: An Overview and Suggested Use of Existing Model Reduction and Experimental System Identification Tools," *IEEE Transactions on Components, Parts and Manufacturing Technology*, vol. 26, pp. 165-172, 2003.

[29] J. Rambo, "Reduced-Order Modeling of Multiscale Turbulent Convection: Application to Data Center Thermal Management," vol. Ph.D. thesis. Atlanta, Georgia: The Georgia Institute of Technology, 2006.

[30] S. Narasimhan, A. Bar-Cohen, and R. Nair, "Thermal Compact Modeling of Parallel Plate Heat Sinks," *IEEE Transaction on Components and Packaging Technologies*, vol. 26, pp. 136-146, 2003.

[31] S. Narasimhan, A. Bar-Cohen, and R. Nair, "Flow and Pressure Field Characteristics in the Porous Block Compact Modeling of Parallel Plate Heat Sinks," *IEEE Transaction on Components and Packaging Technologies*, vol. 26, pp. 147-157, 2003.

[32] W. C. Khedari and J. Hirunlabh, "An Electro-thermal Model of Thermoelectric Modules in Heat Pump and Cooling Mode (CHIM Model)," presented at 20th International Conference on Thermoelectrics, Beijing, China, 2001.

[33] P. E. Bagnoli, C. Casarosa, M. Ciampi, and E. Dallago, "Thermal Resistance Analysis by Induced Transient (TRAIT) Method for Power Electronic Devices Thermal Characterization----Part I: Fundamentals and Theory," *IEEE Transactions on Power Electronics*, vol. 13, pp. 1208-1219, 1998.

[34] Z. Luo, H. Ahn, and M. A. E. Nokali, "A Thermal Model for Insulated Gate Bipolar Thansistor Module," *IEEE Transactions on Power Electronics*, vol. 19, pp. 902-907, 2004.

[35] M. Rencz, G. Farkas, V. Szekely, A. Poppe, and B. Courtois, "Boundary Condition Independent Dynamic Compact Models of Packages and Heat Sinks from Thermal Transient measurements," presented at Electronics Packaging Technology, 2003 5th Conference, Singapore 2003.

[36] R. Hocine, D. Lim, S. H. Pulko, M. A. B. Stambouli, and A. Saidane, "A Three-Dimensional Transmission Line Matrix (TLM) Simulation Method for Thermal Effects in High Power Insulated Gate Bipolar Transistors," *Circuit World*, vol. 29, pp. 27-32, 2003.

[37] W. Habra, P. Tounsi, F. Madrid, P. Dupuy, C. Barbot, and J. M. Dorkel, "A New Methodology for Extraction of Dynamic Compact Thermal Models," presented at 13th International Workshop on Thermal Investigation of ICs and Systems, THERMINIC, Budapest, Hungary, 2007.

[38] P. Holmes, J. L. Lumley, and G. Berkooz, *Turbulence, Coherent Structures*. Cambridge, Great Britain: Cambridge University Press, 86-127, 1996.

[39] A. E. Deane, I. G. Kevrekidis, G. E. Karniadakis, and S. A. Orszag, "Low-Dimensional Models for Complex Geometry Flows: Application to Grooved Channels and Circular Cylinders," *Physics of Fluids A*, vol. 3, pp. 2337-2354, 1991.

[40] X. Ma and G. E. Karniadakis, "A Low-Dimensional Model for Simulating Three-Dimensional Cylinder Flows," *Journal of Fluid Mechanics*, vol. 458, pp. 181-190, 2002.

[41] C. W. Rowley, T. Colonius, and R. M. Murray, "Model Reduction for Compressible Flows Using POD and Galerkin Projection," *Physica D*, vol. 189, pp. 115-129, 2004.

[42] H. M. Park and D. H. Cho, "The Use of the Karhunen-Loeve Decomposition for the Modeling of Distributed Parameter Systems," *Chemical Engineering Science*, vol. 51, pp. 81-98, 1996.

[43] L. Sirovich and H. M. Park, "Turbulent Thermal Convection in a Finite Domain: Part I. Theory," *Physics of Fluids*, vol. 2, pp. 1649-1657, 1990.

[44] I. H. Tarman and L. Sirovich, "Extensions of Karhunen-Loeve Based Approximations of Complicated Phenomena," *Computer Methods in Applied Mechanics and Engineering*, vol. 155, pp. 359-368, 1998.

[45] H. M. Park and W. J. Li, "Boundary Optimal Control of Natural Convection by Means of Mode Reduction," *Journal of Dynamic Systems, Measurement and Control*, vol. 124, pp. 47-54, 2002.

[46] S. S. Ravindran, "Control of Flow Separation over a Forward-Facing Step by Model Reduction," *Computer Methods in Applied Mechanics and Engineering*, vol. 191, pp. 4599-4617, 2002.

[47] H. M. Park and O. Y. Kim, "Reduction of Modes for the Control of Viscous Flows," *International Journal of Engineering Science*, vol. 39, pp. 177-200, 2001.

[48] H. M. Park and W. S. Jung, "The Karhunen-Loeve Galerkin Method for the Inverse Natural Convection Problems," *International Journal of Heat and Mass Transfer*, vol. 44, pp. 155-167, 2001.

[49] D. Rempfer, "On Low-Dimensional Galerkin Models for Fluid Flow," *Theoretical and Computational Fluid Dynamics*, vol. 14, pp. 75-88, 2000.

[50] S. S. Ravindran, "A Reduced-order Approach to Optimal Control of Fluids Using Proper Orthogonal Decomposition," *International Journal for Numerical Methods in Fluids*, vol. 34, pp. 425-448, 2000.

[51] L. Sirovich and I. H. Tarman, "Extensions to Karhunen-Loeve Based Approximations of Complicated Phenomena," *Computer Methods in Applied Mechanics and Engineering*, vol. 155, pp. 359-368, 1998.

[52] H. V. Ly and H. T. Tran, "Modeling and Control of Physical Processes Using Proper Orthogonal Decomposition," *Mathematical and Computer Modeling*, vol. 33, pp. 223-236, 2001.

[53] B. Galletti, C. H. Bruneau, L. Zannetti, and A. Iollo, "Low-Order Modeling of Laminar Flow Regimes Past a Confined Square Cylinder," *Journal of Fluid Mechanics*, vol. 503, pp. 161-170, 2004.

[54] J. Rambo and Y. Joshi, "Reduced-Order Modeling of Turbulent Forced Convection With Parametric Conditions," *International Journal of Heat and Mass Transfer*, vol. 50, pp. 539-551, 2007.

[55] B. Shapiro, "Creating Reduced-Order Models for Electronic Systems: An Overview and Suggested Use of Existing Model Reduction and Experimental System Identification Tools," presented at Thermal Challenges in Next Generation Electronic Systems: Thermes, Millpress, Netherlands, 2002.

[56] Q. Nie and Y. Joshi, "Reduced Order Modeling and Experimental Validation of Steady Turbulent Convection in Connected Domains," *International Journal of Heat and Mass Transfer*, vol. in press, 2008.

[57] Q. Nie and Y. Joshi, "Multiscale Thermal Modeling of Power Electronic Cabinet with Double-Sided Cooling," presented at Itherm, Orlando, USA 2008.

[58] A. Bar-Cohen and W. Krueger, "Thermal Characterization of Chip Packages - Evolutionary Design of Compact Models," *IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part A*, vol. 20, pp. 399-410, 1997.

[59] C. J. M. Lasance, "Special Section on Compact Thermal Modeling," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, pp. 134-135, 2003.

[60] C. J. M. Lasance, "Highlights from the European Thermal Project PROFIT," *ASME Journal of Electronic Packaging*, vol. 126, pp. 565-570, 2004.

[61] C. J. M. Lasance, H. I. Rosten, and J. D. Parry, "The World of Thermal Characterization According to DELPHI - Part II: Experimental and Numerical Methods," *IEEE Transactions on Components, Packaging, and manufacturing Technology - Part A*, vol. 20, pp. 392-398, 1997.

[62] H. I. Rosten, C. J. M. Lasance, and J. D. Parry, "The World of Thermal Characterization According to DELPHI - Part I: Background to DELPHI," *IEEE Transactions on Components, Packaging, and manufacturing Technology - Part A*, vol. 20, pp. 384-391, 1997.

[63] M. Brajtman, P. Gunupudi, D. Celo, T. Smy, and M. Nakhla, "Fast Thermal Transient Analysis and Macro-model Creation,," presented at 10th International

Workshop on Thermal Investigations of ICs and Systems, Therminic, Sophia Antipolis, France, 2004.

[64] L. Feng, E. B. Rudnyi, and J. G. Korvink, "Boundary Condition Independent Compact Thermal Model," presented at 10th International Workshop on Thermal Investigations of ICs and Systems, Therminic Sophia Antipolis, France, 2004.

[65] X. Guo, D. Celo, D. J. Walkey, and T. Smy, "The Use of Constant Heat Flow Ports For Thermal Macro-models," presented at 10th International Workshop on Thermal Investigations of ICs and Systems, Therminic, Sophia Antipolis, France, 2004.

[66] E. Zukowski, J. Wilde, E. B. Rudnyi, and J. G. Korvink, "Model Reduction For Thermo-Mechanical Simulation of Packages," presented at 11th International Workshop on Thermal Investigations of ICs and Systems, Therminic, Belgirate, Italy, 2005.

[67] J. Rambo and Y. Joshi, "Multi-Scale Modeling of High Power Density Data Centers," presented at The Pacific Rim / ASME International Electronics Packaging Technical Conference and Exhibitio, Kauai, HI, 2003.

[68] Q. Nie and Y. Joshi, "Multiscale Thermal Modeling Methodology for Electronic Cabinets," presented at Proceedings of ITHERM'06, 2006.

[69] B. Kader, "Temperature and Concentration Profiles in Fully Turbulent Boundary Layers," *International Journal of Heat and Mass Transfer*, vol. 24, pp. 1541-1544, 1981.

[70] L. Sirovich, "Turbulence and Dynamics of Coherent Structures, Part I - III," *Quarterly of Applied Mathematics*, vol. XLV (3), pp. 561-590, 1987.

[71] E. A. Christensen, M. Brons, and J. N. Sorensen, "Evaluation of Proper Orthogonal Decomposition - Based Techniques Applied to Parameter Dependent Nonturbulent Flows," *SIAM Journal of Scientific Computing*, vol. 21, pp. 1419-1434, 2000.

[72] Enertron, *Thermoelectric Cooling - The Basics*. Enertron Inc, Arizona: Enertron Inc Online Source, 2000.

[73] G. Peng and M. Ishizuka, "Numerical Simulation of Heat Dissipation from a Plastic Ball Grid Array Package in a Thin Flat Box: Effects of Some Operative and Geometric Parameters," *Numerical Heat Transfer, Part A*, vol. 45, pp. 67-83, 2004.

[74] L. Tang and Y. Joshi, "Multiscale Conjugate Thermal Modeling Approach for Air Cooled Electronic Enclosures," *ASEM EEP*, vol. 26, pp. 295-304, 1999.

[75] L. Tang and Y. Joshi, "A Multi-grid Based Multi-scale Thermal Analysis Approach for Combined Mixed Convection, Conduction and Radiation Due to Discrete Heating," *J. Heat Transfer*, vol. 127, pp. 18-26, 2005.

[76] H. I. Rosten, J. D. Parry, J. S. Addison, R. Viswanath, and E. Fitzgrald, "Development, Validation and Application of a Thermal Model of a Plastic Quad Flat Pack," presented at Proc. 45th Electronic Component and Technology Conference, 1995.

[77] Y. Utturkar, B. Zhang, and W. Shyy, "Reduced-Order Description of Fluid Flow with Moving Boundaries by Proper Orthogonal Decomposition," *International Journal of Heat and Fluid Flow*, vol. 26, pp. 276-288, 2005.

[78] C. Belady, K. M. Kelkar, and S. V. Patankar, "Improving Productivity in Electronic Packaging with Flow Network Modeling (FNM)," *Electronics Cooling*, vol. 5, pp. 36-40, 1995.

[79] B. Lian, T. Dishongh, D. Pullen, H. Yan, and J. Chen, "Flow Network Modeling for Improving Flow Distribution of Microelectronics Burn-In-Oven," presented at The 7th Intersociety Conference on Thermal and Mechanical Phenomena in Electronic Systems, Las Vegas, NV, 2000.

[80] I. E. Idelchik, *Handbook of Hydraulic Resistance*, vol. 8.1-8.30. Florida: CRC Press, 1994.

[81] S. V. Patankar, *Numerical Heat Transfer and Fluid Flow*. MacGraw Hill, New York, 121-135, 1980.

[82] S. P. Vanka, "Block-implicit Multi-grid Solution of Navier-Stokes Equations in Primitive Variables," *J. Computational Physics*, vol. 65, pp. 38-158, 1986.

[83] M. Hernandez-Mora, J. E. Gozalez, M. Velez-Reyes, J. M. Ortiz-Rodriguez, Y. Pang, and E. Scott, "Dynamic Reduced Electrothermal Model for Integrated Power Electronics Modules (IPEM)," *ASME J. Electronics Packaging*, vol. 126, pp. 477-490, 2004.

[84] G. Ellison, "Maximum Thermal Spreading Resistance for Rectangular Sources and Plates With Nonunity Aspect Ratios," *IEEE Trans. Comp., Hybrids, Manufac. Technol.*, vol. 26, 2003.

[85] V. Heinz and J. M. Lasance, "Compact Models for Accurate Thermal Characterization of Electronic Parts, IEEE Transactions on Components," *Packaging, and Manufacturing Technology. Part A*, vol. 20, pp. 411-419, 1997.

[86] A. Bar-Cohen, T. Elperin, and R. Eliasi, "Characterization of Chip Packages Justifications, Limitations and Future," *IEEE Transaction on Components, Hybrids, and Manufacturing Technology*, vol. 12, pp. 724-731, 1989.

[87] C. Lasance, "Two Benchmarks to Facilitate the Study of Compact Thermal Modeling Phenomena," *IEEE Transactions on Components and Packaging Technologies*, vol. 24, pp. 559-565, 2001.

[88] S. Lee, S. Song, V. Au, and K. Moran, "Constriction/Spreading Resistance Model for Electronic Packaging," presented at Proceedings of ASME/JSME Engineering Conference, 1995.

[89] M. Yovanovich, Y. Muzychka, and J. Culham, "Spreading Resistnace of Isoflux Rectangules and Strips on Compound Flux Channels," University of Waterloo, 1998.

[90] R. Simons, "Simple Formulas for Estimating Therma Spreading Resistance," *Electronics Cooling*, 2004.

[91] "www.cfdesign.com/pdf_files/tech-report-thermal-resistance.pdf," [accessed July 1, 2008].

[92] J. V. Reichl, "Inverter Dynamics Electro-Thermal Simulations with Experimental Verification," vol. MSEE: Virginia Institute of Technology, 2005.

[93] S. S. Ravindran, "Adaptive Reduced-Order Controllers for a Thermal Flow Using Proper Orthogonal Decomposition," *SIAM Journal of Scientific Computing*, vol. 23, pp. 1924-1942, 2002.

[94] I. Mudawar, "Assessment of High-Heat-Flux Thermal Management Schemes," *Components and Packaging Technologies, IEEE Transactions on*, vol. 24, pp. 122-141, 2001.

[95] T. Steiner and R. Sittig, "IGBT Module Setup with Integrated Micro-Heatsinks," presented at Power Semiconductor Devices and ICs, The 12th International Symposium on, 2000.

[96] C. Gillot, C. Schaeffer, C. Massit, and L. Meysenc, "Double-sided Cooling for High Power IGBT Modules Using Flip Chip Technology," *Components and Packaging Technologies, IEEE Transactions on*, vol. 24, pp. 698-704, 2001.

[97] J. Yin, J. D. v. Wyk, W. G. Odendaal, and Z. Liang, "Design and Optimization of Embedded Power Chip Module for Double-Sided Cooling," presented at Industry Applications Conference, 39th IAS Annual Meeting, 2004.

[98] B. C. Charboneau, F. Wang, J. D. v. Wyk, D. Boroyevich, Z. Liang, and E. P. Scott, "Double-Sided Cooling for Power Semiconductor Devices Using Embedded Power Packaging," presented at Industry Applications Conference, 40th IAS Annual Meeting, 2006.

[99] L. Burton, "Multiscale Thermal Modeling Methodology for High Power Electronic Cabinet," Georgia Institute of Technology, 18-52, 2007.

[100] T. R. Kuphaldt, "Kelvin (4-wire) Resistance Measurement," All About Circuits: Volume I—DC, 2003, [accessed August 9, 2008], http://www.allaboutcircuits.com/vol_1/chpt_8/9.html.

[101] M. Kaviany, *Principal of Heat Transfer in Porous Medium, 2nd ed*. New York: Springer-Verlag, 100-150, 1995.

[102] S. Kakac and H. Liu, *Heat Exchanger: Selection, Rating, and Thermal Design*: CRC Press, 2002.

[103] "http://www.curamik.com/sprache2/n160352/i230562.html," [accessed June 25, 2008].

[104] M. Rathnam and L. R. Petzold, "Dynamic Iteration Using Reduced Order Models: A Method for Simulation of Large Scale Modular System," *SIAM Journal of Numerical Analysis*, vol. 40, pp. 1446-1474, 2003.

[105] M. D. Graham and I. G. Kevrekidis, "Alternative Approaches to the Karhunen-Loeve Decomposition for Model Reduction and Data Compression," *Computers in Chemical Engineering*, vol. 20, pp. 495-506, 1996.

[106] G. Nelson, "Development of An Experimentally-Validated Compact Model of A Server Rack," in *School of Mechanical Engineering*, vol. M.S.: Georgia Institute of Technology, 2007.